EXAMINED BY： Dan Kao	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO. CAS-P00888
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		VERSION：P

CUSTOMER ACCEPTANCE SPECIFICATIONS

MODEL NO. :

EIML101022DYA

(RoHS)

FOR MESSRS :

CUSTOMER'S APPROVAL

DATE：

_____

BY：

_____

RECORDS OF REVISION

DOC. FIRST ISSUE

NOV.24, 2023

DATE	REVISED PAGE NO.	SUMMARY

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1. GENERAL SPECIFICATIONS

1.1 DATA SHEETS FOR CONTROLLER / DRIVER PLEASE REFER TO：

ILI 9882T OR EQUIVALENT

1.2 MATERIAL SAFETY DESCRIPTION
ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED
DIPHENYL ETHERS (PBDE), BIS(2-ETHYLHEXYL) PHTHALATE (DEHP), BUTYL BENZYL PHTHALATE (BBP), DIBUTYL PHTHALATE (DBP), DIISOBUTYL PHTHALATE (DIBP).

2. MECHANICAL SPECIFICATIONS

2.1 TFT LCD MODULE MECHANICAL SPECIFICATIONS

(1)	DISPLAY SIZE	10.1 inch
(2)	NUMBER OF DOTS	1200(RGB)W * 1920H DOTS
(3)	MODULE SIZE	140.66W * 226.61H * 8.7D(MAX.) mm
(4)	ACTIVE AREA	135.36W * 216.576H mm
(5)	DOT SIZE	0.0376W * 0.1128H mm
(6)	PIXEL SIZE	0.1128W * 0.1128H mm
(7)	LCD TYPE	TFT, IPS, TRANSMISSIVE, NORMALLY BALCK
(8)	COLOR	16.7M
(9)	VIEWING DIRECTION	SUPER WIDE VIEW
(10)	BACK LIGHT	LED , COLOR : WHITE
(11)	INTERFACE MODE	MIPI
(12)	WEIGHT	TBD

2.2 CAPACITIVE TOUCH PANEL MECHANICAL SPECIFICATIONS

(1) TOUCH PANEL SIZE ---------- 10.1 inch
(2) OUTER DIMENSION ---------- 140.66W * 226.61H mm
(3) ACTIVE AREA ---------- 135.36W * 216.576H mm
(4) INPUT TYPE ---------- MULTI TOUCH
(5) NUMBER OF TOUCH SENSOR ---------- 32*48 SENSORS
(6) RESOULTION ---------- 1200 * 1920
(7) INTERFACE MODE ---------- I2C
(8) THE MATERIAL OF COVER LENS ---------- GLASS

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE	VDD-VSS	-0.3	1.95	V	—
	AVDD-VSS	-0.3	6.3	V	—
	AVEE-VSS	-6.3	0.3	V	—
POWER DISSIPATION FOR LED BACKLIGHT	PD	—	(9900)	mW	—
FORWARD CURRENT FOR LED BACKLIGHT	ILED	—	(600)	mA	—
STATIC ELECTRICITY	—	—	—	V	NOTE (1)

NOTE (1)：LCM SHOULD BE GROUND DURING LCM HANDLING.

NOTE (2)：THE ABSOLUTE MAXIMUM RATING VALUES OF THIS PRODUCT ARE NOT ALLOWED TO BE EXCEEDED AT ANY TIMES. SHOULD A MODULE BE USED WITH ANY OF THE ABSOLUTE MAXIMUM RATINGS EXCEEDED, THE CHARACTERISTICS OF THE MODULE MAY NOT BE RECOVERED, OR IN AN EXTREME CASE, THE MODULE MAY BE PERMANENTLY DESTROYED.

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	(-20°C)	(70°C)	-20°C	70°C	NOTE (1),(2),(3),(4)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
VIBRATION	—	2.45 m/s^2 (0.25 G)	—	11.76 m/s^2 (1.2 G)	10~100 Hz XYZ DIRECTIONS 1 HR EACH
SHOCK	—	29.4 m/s^2 (3 G)	—	490 m/s^2 (50 G)	10 ms XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (1)：THE ABSOLUTE MAXIMUM RATINGS OF THIS PRODUCT SHOULD NOT BE EXCEEDED AT ANY TIME. IF THESE RATINGS ARE EXCEEDED, THE PRODUCT'S PERFORMANCE IS NOT GUARANTEED AND THE PRODUCT MAY EXPERIENCE PERMANENT DAMAGE.

NOTE (2)：BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (3)：Ta ≤ 60°C：90% RH MAX. (96HRS MAX).
Ta > 60°C：ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90% RH AT 90°C(96 HRS MAX).

NOTE (4)： WHEN THE LCD MODULE IS OPERATED AT A HIGHER AMBIENT TEMPERATURE THAN 60°C, THE PWM DUTY CYCLE OF THE LED BACKLIGHT SHOULD BE ADJUSTED TO BE LESS THAN TBD%. IF THE MODULE IS OPERATED AT A HIGHER DUTY CYCLE THAN TBD, THEN THERE IS A POSSIBILITY OF DISTORTION AND IRREGULARITY OF THE PICTURE DUE TO LIQUID CRYSTAL BEHAVIOR.

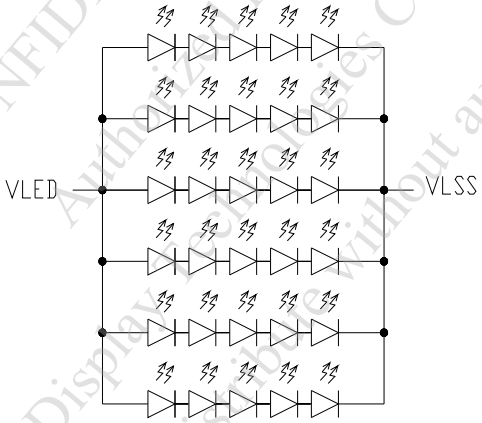
4. ELECTRICAL CHARACTERISTICS

Ta = 25 °C

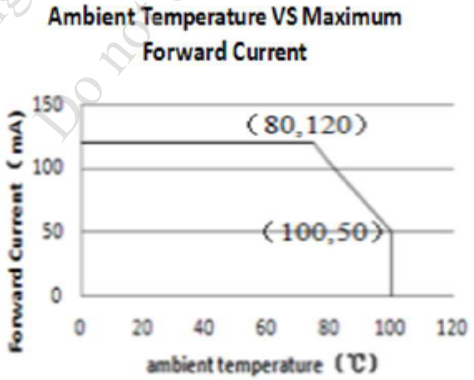
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE	VDD-VSS	—	(1.65)	(1.80)	(1.95)	V	
POWER SUPPLY VOLTAGE FOR CIRCUITS	AVDD -VSS	—	(4.5)	(5.5)	(6.3)	V	
	AVEE -VSS	—	(-6.3)	(-5.5)	(-4.5)	V	
POWER SUPPLY CURRENT	IDD	VDD-VSS=(1.80)V	—	TBD	TBD	mA	NOTE (1)
POWER SUPPLY CURRENT FOR CIRCUITS	IAVDD	AVDD-VSS=(5.0)V	—	TBD	TBD	mA	
	IAVEE	AVEE-VSS=(-5.0)V	—	TBD	TBD		
POWER SUPPLY VOLTAGE FOR LED BACKLIGHT	VLED-VLSS	IF=(600)mA	14	TBD	16.5	V	
LED LIFE TIME	—	(I_{LED}=80mA) (PER LED)	(50K)	—	—	HRS	NOTE (4) NOTE (5)

NOTE (1)：THE DISPLAY PATTERN IS ALL “WHITE”.

NOTE (2)：INTERNAL CIRCUIT DIAGRAM OF BACKLIGHT



NOTE (3)：AMBIENT TEMP. VS. ALLOWABLE FORWARD CURRENT.(PER LED)



NOTE (4)：CONDITIONS; TA=25 °C, CONTINUOUS LIGHTING.

NOTE (5)：DEFINITIONS OF LIFE TIME
LCD LUMINANCE BECOMES HALF OF THE INITIAL VALUE.

5. TIMING CHARACTERISTICS

5.1 FOR LCD MODULE

5.1.1 DC CHARACTERISTICS FOR PANEL DRIVING

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POWER & OPERATION VOLTAGE						
LOGIC OPERATING VOLTAGE	IOVCC	—	1.65	1.8	1.95	V
OPERATING VOLTAGE	AVDD	—	4.5	5.5	6.3	V
OPERATING VOLTAGE	AVEE	—	-6.3	-5.5	-4.5	V
LOGIC OPERATING VOLTAGE	VDDAM	—	1.65	1.8	1.95	V
LOGIC HIGH LEVEL INPUT VOLTAGE	V_{IH}	—	0.7* VDD	—	VDD	V
LOGIC LOW LEVEL INPUT VOLTAGE	V_{IL}	—	0	—	0.3* VDD	V
LOGIC HIGH LEVEL OUTPUT VOLTAGE TE, LEDPWM	V_{OH}	I_{OH}=-1.0mA	0.8* VDD	—	VDD	V
LOGIC LOW LEVEL OUTPUT VOLTAGE TE, LEDPWM	V_{OL}	I_{OH}=+1.0mA	0	—	0.2* VDD	V
DRIVER SUPPLY VOLTAGE	—	—	—	—	32	V
VCOM OPERATION						
DC VCOM AMPLITUDE VOLTAGE	VCOM	—	-4.0	—	0	V
SOURCE DRIVERG						
POSITIVE SOURCE OUTPUT RANGE	V_{SOUT}	—	0.2	—	GVDDP	V
NEGATIVE SOURCE OUTPUT RANGE	V_{SOUT}	—	GVDDN	—	-0.2	V
POSITIVE GAMMA REFERENCE VOLTAGE	GVDDP	—	3	—	6	V
NEGATIVE GAMMA REFERENCE VOLTAGE	GVDDN	—	-6	—	-3	V
SOURCE OUTPUT SETTING TIME	Tr	BELOW WITH 99% PRECISION	—	3.5		us
SOURCE OUTPUT DEVIATION VOLTAGE	V_{DEV}	|SOUT|>=4.2V |SOUT|<=0.8V	—	20	30	mV
		4.2V>|SOUT|>0.8V		10	15	mV
SOURCE OUTPUT OFFSET VOLTAGE	V_{OFFSET}	—	—	4		mV
BOOSTER OPERATION3						
GATE DRIVER HIGH VOLTAGE	VGHO	—	3	—	20	V
GATE DRIVER LOW VOLTAGE	VGLO	—	-3	—	-16	V
CHARGE PUMP HIGH VOLTAGE	VGH		6	—	20	
CHARGE PUMP LOW VOLTAGE	VGL		-6	—	-16	
HALF AVDD CHARGE PUMP	VCIP			1/2* AVDD		

5.1.2 DC CHARACTERISTICS FOR DSI LP MODE

DC LEVELS OF THE LP-00, LP-01, LP-10 AND LP-11 ARE DEFINED ON TABLE BELOW. DC CHARACTERISTICS FOR DSI LP MODE WHEN LP-RX, LP-CD OR LP-TX IS MENTIONED ON THE CONDITION COLUMN.

ITEM	SYMBOL	CONDITIONS	SPECIFICATION			UNIT
			MIN.	TYP.	MAX.	
LOGIC HIGH LEVEL OUTPUT VOLTAGE	V_{OHLP}	IOUT = -1mA	0.8* VDDAM	—	VDDAM	V
LOGIC LOW LEVEL OUTPUT VOLTAGE	V_{OLLP}	IOUT = 1mA	0.0	—	0.2* VDDAM	V
LOGIC HIGH LEVEL INPUT VOLTAGE	V_{IHLPCD}	LP-CD	450	—	1350	mV
LOGIC LOW LEVEL INPUT VOLTAGE	V_{ILLPCD}	LP-CD	0.0	—	200	mV
LOGIC HIGH LEVEL INPUT VOLTAGE	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	—	1350	mV
LOGIC LOW LEVEL INPUT VOLTAGE	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0.0	—	550	mV
LOGIC LOW LEVEL INPUT VOLTAGE	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	—	300	mV
LOGIC HIGH LEVEL OUTPUT VOLTAGE	V_{OHLPTX}	LP-TX (D0)	1.1	—	1.3	V
LOGIC LOW LEVEL OUTPUT VOLTAGE	V_{OLLPTX}	LP-TX (D0)	-50	—	50	mV
LOGIC HIGH LEVEL INPUT CURRENT	I_{IH}	LP-CD, LP-RX	—	—	10	uA
LOGIC LOW LEVEL INPUT CURRENT	I_{IL}	LP-CD, LP-RX	-10	—	—	uA

5.1.3 DC CHARACTERISTICS FOR DSI HS MODE

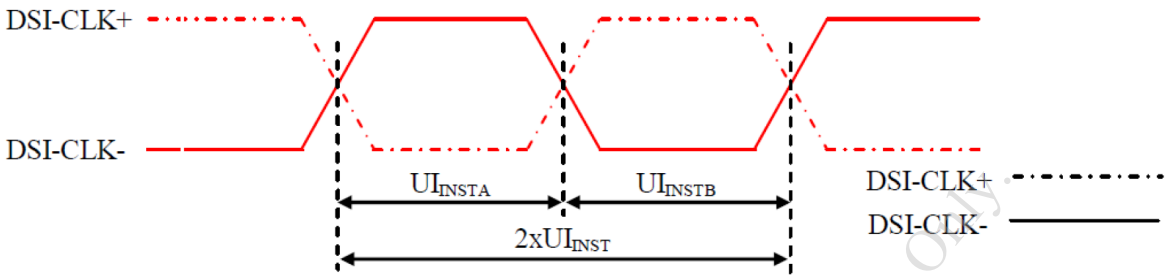
ITEM	SYMBOL	CONDITIONS	SPECIFICATION			UNIT
			MIN.	TYP.	MAX.	
INPUT COMMON MODE VOLTAGE FOR CLOCK	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	—	330	mV
INPUT COMMON MODE VOLTAGE FOR DATA	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	—	330	mV
COMMON MODE RIPPLE FOR CLOCK EQUAL OR LESS THAN 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	—	50	mV
COMMON MODE RIPPLE FOR DATA EQUAL OR LESS THAN 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	—	50	mV
COMMON MODE RIPPLE FOR CLOCK MORE THAN 450MHz (PEAK SINE WAVE)	$V_{CMRCLKM450}$	DSI-CLK+/-	—	—	100	mV
COMMON MODE RIPPLE FOR DATA MORE THAN 450MHz (PEAK SINE WAVE)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	—	—	100	mV
DIFFERENTIAL INPUT LOW LEVEL THRESHOLD VOLTAGE FOR CLOCK	$V_{THLCLK-}$	DSI-CLK+/-	-70	—	—	mV
DIFFERENTIAL INPUT LOW LEVEL THRESHOLD VOLTAGE FOR DATA	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	—	—	mV
DIFFERENTIAL INPUT HIGH LEVEL THRESHOLD VOLTAGE FOR CLOCK	$V_{THHCLK+}$	DSI-CLK+/-	—	—	70	mV
DIFFERENTIAL INPUT HIGH LEVEL THRESHOLD VOLTAGE FOR DATA	$V_{THHDATA+}$	DSI-Dn+/- Note 5	—	—	70	mV
SINGLE-ENDED INPUT LOW VOLTAGE	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	—	—	mV
SINGLE-ENDED INPUT HIGH VOLTAGE	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	—	—	460	mV
DIFFERENTIAL TERMINATION RESISTOR	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
SINGLE-ENDED THRESHOLD VOLTAGE FOR TERMINATION ENABLE	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	—	—	450	mV
TERMINATION CAPACITOR	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	—	—	60	pF

NOTE(1): Ta = -30 TO 70˚C (TO +85°C NO DAMAGE), VDD=1.65V~1.95V, AVDD=4.5V~6.6V, AVEE=-4.5V~-6.6V,VSS=AVSS=0V.
NOTE(2): INCLUDES 50mV (-50mV to 50mV) GROUND DIFFERENCE.
NOTE(3): WITHOUT VCMRCLKM450/VCMRDATAM450.
NOTE(4): WITHOUT 50mV (-50mV to 50mV) ground difference.
NOTE(5): n = 0,1,2,3
NOTE(6): FOR HIGHER BIT RATES A 14pF CAPACITOR WILL BE NEEDED TO MEET THE COMMON-MODE RETURN LOSS SPECIFICATION.

5.2 AC CHARACTERISTICS

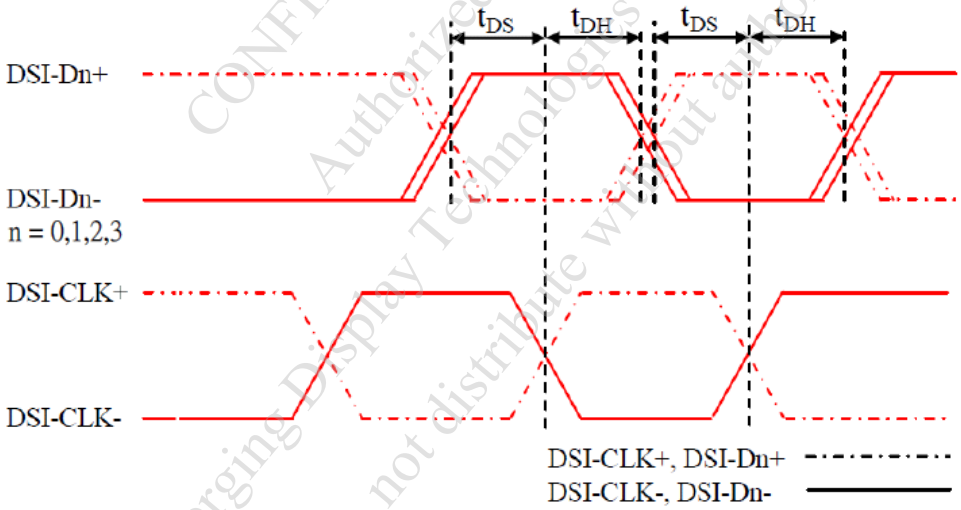
5.2.1 DSI TIMING CHARACTERISTICS

5.2.1.1 HIGH SPEED MODE – CLOCK CHANNEL TIMING



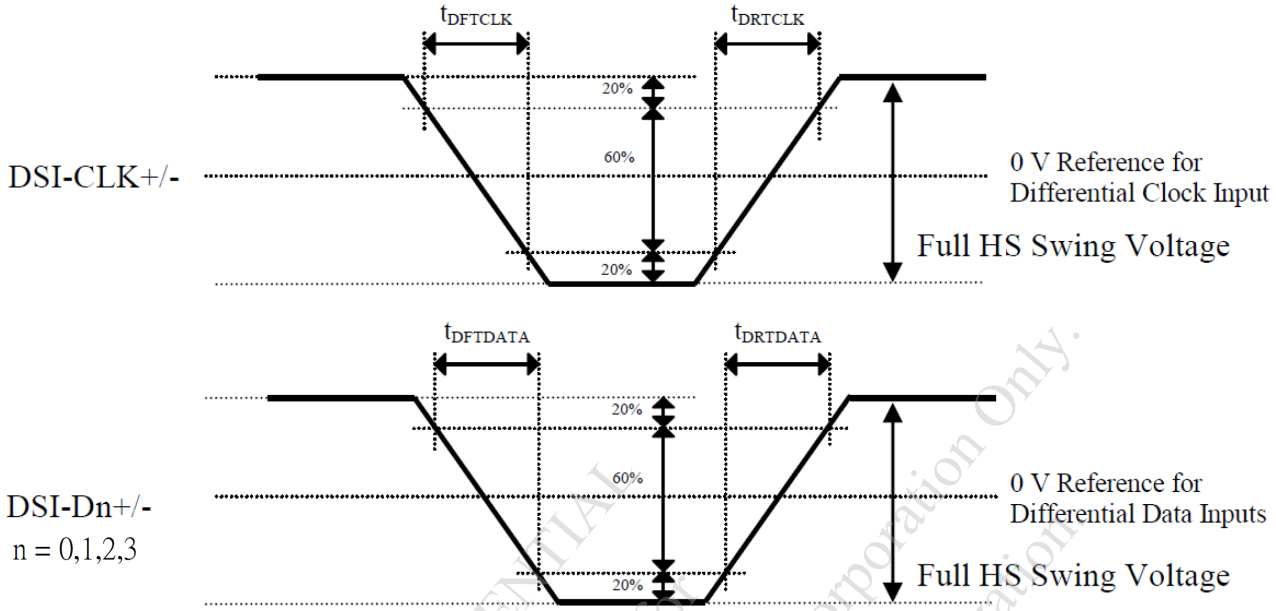
ITEM	SIGNAL	SYMBOL	MIN.	MAX.	UNIT
DOUBLE UI INSTANTANEOUS	DSI-CLK+/-	2xUiinst	1.66	25	Ns
UI INSTANTANEOUS HALF	DSI-CLK+/-	Uiinsta,Uiinstb	0.83	12.5	ns

5.2.1.2 HIGH SPEED MODE – DATA CLOCK CHANNEL TIMING



ITEM	SIGNAL	SYMBOL	MIN.	MAX.
DATA TO CLOCK SETUP TIME	DSI-Dn+/- (n=0,1,2,3)	t_{DS}	0.15xUI	—
CLOCK TO DATA HOLD TIME		t_{DH}	0.15xUI	—

5.2.1.3 HIGH SPEED MODE – CLOCK CHANNEL TIMING

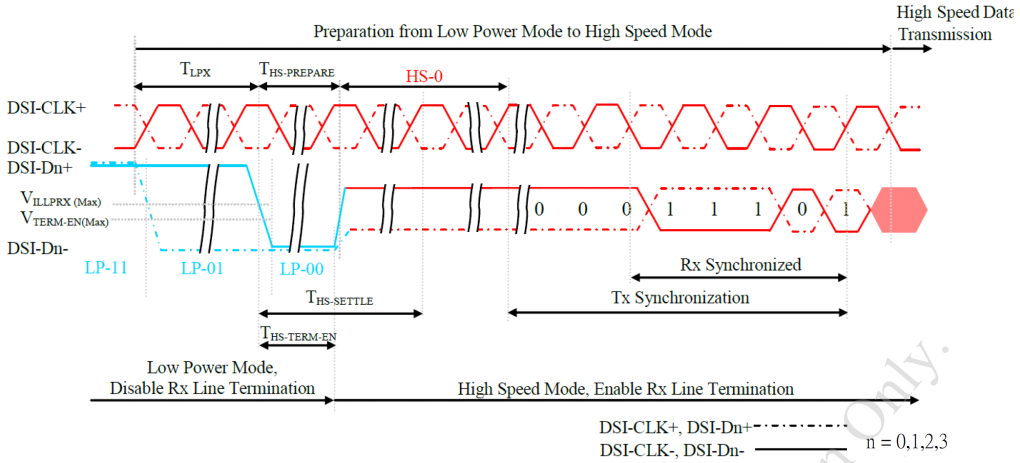


RISE AND FALL TIMINGS ON CLOCK AND DATA CHANNELS

ITEM	SYMBOL	CONDITION	SPECIFICATION		
			MIN.	MAX.	UNIT
DIFFERENTIAL RISE TIME FOR CLOCK	t_{DRTCLK}	DSI-CLK+/-	150 ps	—	0.3UI
DIFFERENTIAL RISE TIME FOR DATA	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	—	0.3UI
DIFFERENTIAL FALL TIME FOR CLOCK	t_{DFTCLK}	DSI-CLK+/-	150 ps	—	0.3UI
DIFFERENTIAL FALL TIME FOR DATA	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	—	0.3UI

NOTE(1): THE DISPLAY MODULE HAS TO MEET TIMING REQUIREMENTS, WHAT ARE DEFINED FOR THE TRANSMITTER (MCU) ON MIPI D-PHY STANDARD.

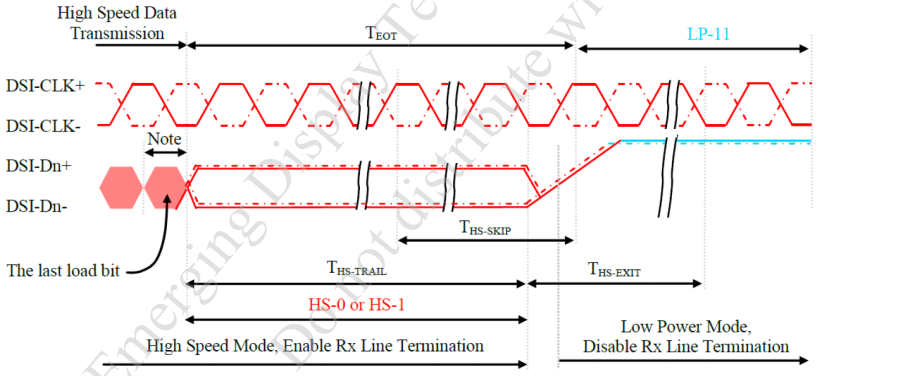
5.2.1.4 DATA LANES FROM LOW POWER MODE TO HIGH SPEED MODE



DATA LANES – LOW POWER MODE TO HIGH SPEED MODE TIMINGS

SIGNAL	SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
DSI-Dn+/- (n=0,1,2,3)	T_{LPX}	LENGTH OF ANY LOW POWER STATE PERIOD	50	—	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-PREPARE}$	TIME TO DRIVE LP-00 TO PREPARE FOR HS TRANSMISSION	40+4XUI	85+6XUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TERM-EN}$	TIME TO ENABLE DATA LANE RECEIVER LINE TERMINATION MEASURED FROM WHEN DN CROSSES VILMAX	—	35+4XUI	ns

5.2.1.5 DATA LANES FROM HIGH SPEED MODE TO LOW POWER MODE

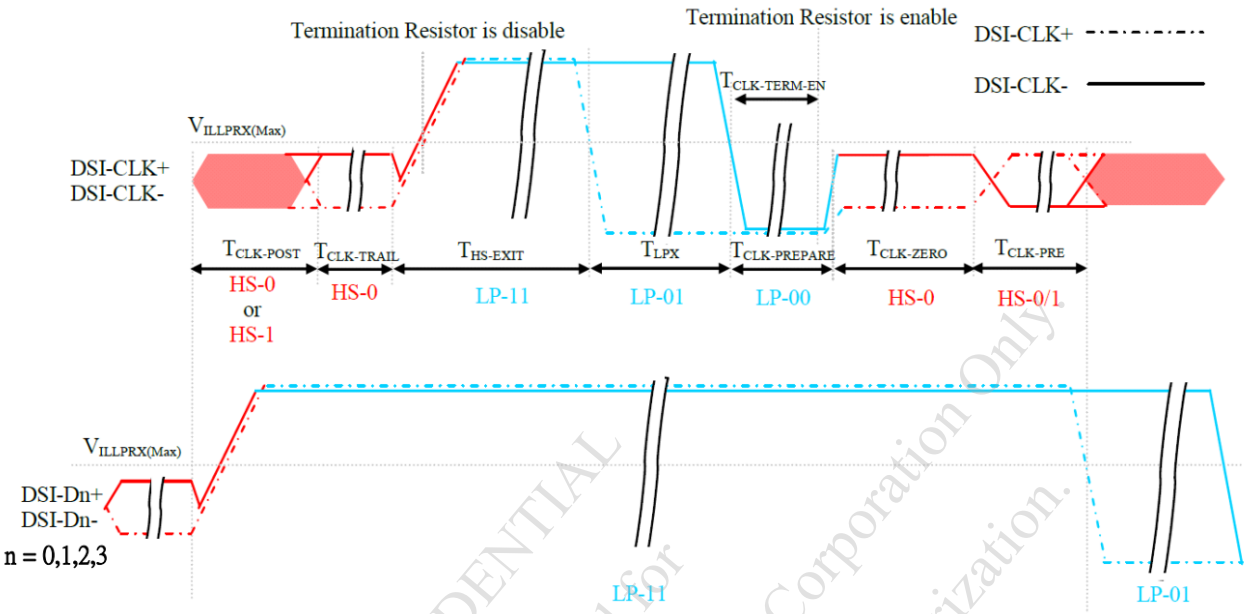


Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

DATA LANES – HIGH SPEED MODE TO LOW POWER MODE TIMINGS

SIGNAL	SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-SKIP}$	TIME-OUT AT DISPLAY MODULE (ILI9882T) TO IGNORE TRANSITION PERIOD OF EOT	40	55+4xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-EXIT}$	TIME TO DRIVER LP-11 AFTER HS BURST	100	—	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TRAIL}$	TIME THAT THE TRANSMITTER DRIVES THE FLIPPED DIFFERENTIAL STATE AFTER LAST PAYLOAD DATA BIT OF A HS TRANSMISSION BURST	max(8*UI, 60ns+ 4*UI)	—	ns

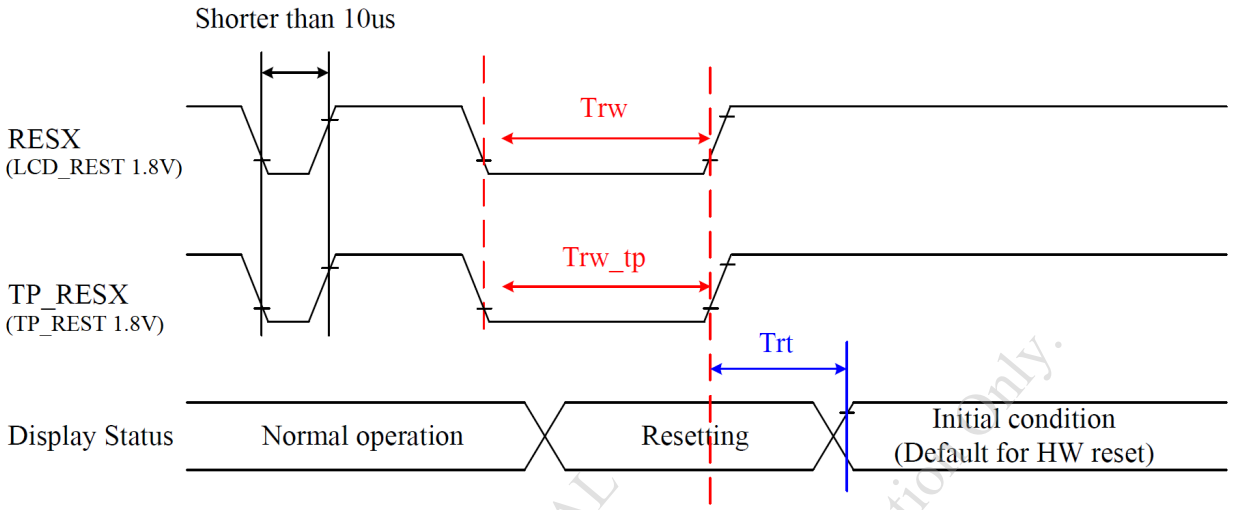
5.2.1.6 DSI CLOCK BURST – HIGH SPEED MODE TO/FROM LOW POWER MODE



CLOCK LANES – HIGH SPEED MODE TO/FROM LOW POWER MODE TIMINGS

SIGNAL	SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
DSI-CLK+/-	$T_{CLK-POST}$	TIME THAT THE MCU SHALL CONTINUE SENDING HS CLOCK AFTER THE LAST ASSOCIATED DATA LANES HAS TRANSITIONED TO LP MODE	60+52xUI	—	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	TIME TO DRIVE HS DIFFERENTIAL STATE AFTER LAST PAYLOAD CLOCK BIT OF A HS TRANSMISSION BURST	60	—	ns
DSI-CLK+/-	$T_{HS-EXIT}$	TIME TO DRIVE LP-11 AFTER HS BURST	100	—	ns
DSI-CLK+/	$T_{CLK-PREPARE}$	TIME TO DRIVE LP-00 TO PREPARE FOR HS TRANSMISSION	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	TIME-OUT AT CLOCK LANE TO ENABLE HS TERMINATION	—	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	MINIMUM LEAD HS-0 DRIVE PERIOD BEFORE STARTING CLOCK	38	—	ns
DSI-CLK+/-	$T_{CLK-PRE}$	TIME THAT THE HS CLOCK SHALL BE DRIVEN PRIOR TO ANY ASSOCIATED DATA LANE BEGINNING THE TRANSITION FROM LP TO HS MODE	8xUI	—	ns

5.3 RESET TIMING



RESET TIMING

ITEM	SIGNAL	SYMBOL	MIN.	MAX.	UNIT
RESET PULSE DURATION	RESX	Trw	10	—	us
RESET CANCEL		Trt	35 (NOTE 1,5)	—	ms
			150 (NOTE 1,6,7)	—	ms
RESET PULSE DURATION	TP_RESX	Trw_tp	10	—	us

NOTE(1) : THE RESET CANCEL INCLUDES ALSO REQUIRED TIME FOR LOADING ID BYTES, VCOM SETTING AND OTHER SETTINGS FROM NVM TO REGISTERS. THIS LOADING IS DONE EVERY TIME WHEN THERE IS H/W RESET CANCEL TIME (TRT) WITHIN 5 MS AFTER A RISING EDGE OF RESX.

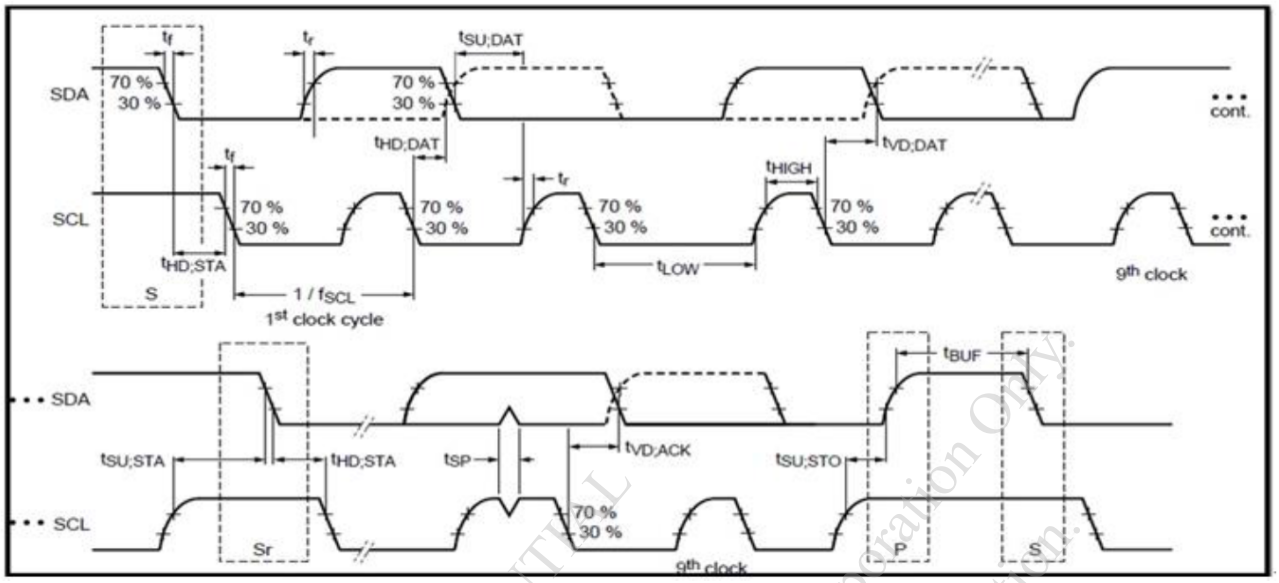
NOTE(2) : SPIKE DUE TO AN ELECTROSTATIC DISCHARGE ON RESX LINE DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE FOLLOWING TABLE.

RESX	Action
SHORTER THAN 5us	RESET REJECTED
LONGER THAN 9us	RESET
BETWEEN 5us AND 9us	RESET STARTS

NOTE(3) : DURING THE RESETTING PERIOD, THE DISPLAY WILL BE BLANKED (THE DISPLAY IS ENTERING BLANKING SEQUENCE, WHICH MAXIMUM TIME IS 120 MS, WHEN RESET STARTS IN SLEEP OUT MODE. THE DISPLAY REMAINS THE BLANK STATE IN SLEEP IN MODE.) AND RETURN TO DEFAULT CONDITION FOR HARDWARE RESET.

NOTE(4) : SPIKE REJECTION ALSO APPLIES DURING A VALID RESET PULSE AS SHOWN IN FOLLOWING FIGURE.

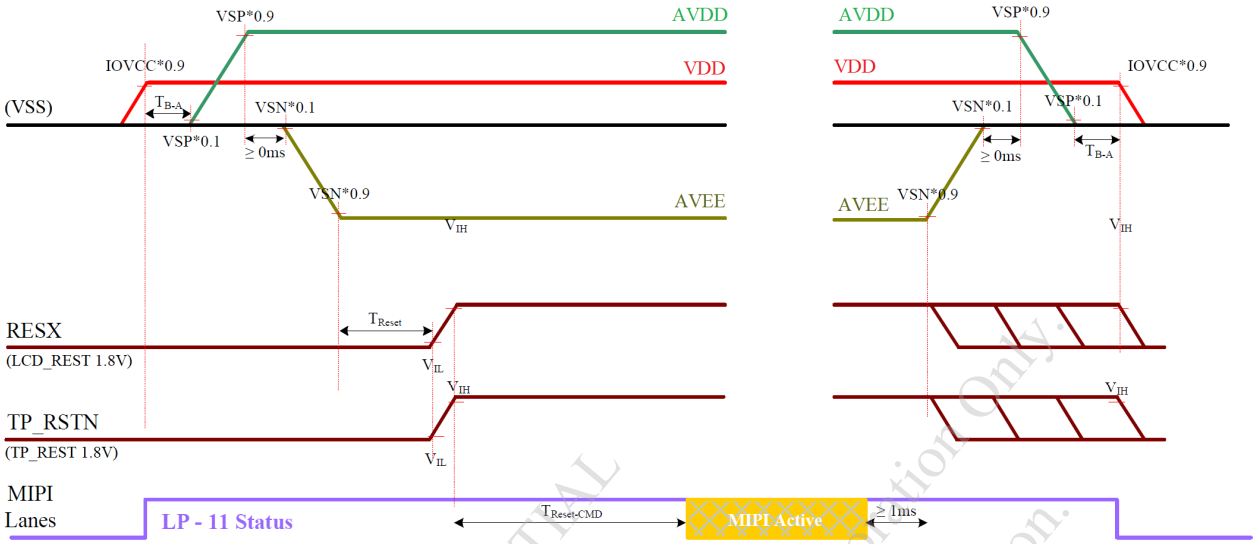
5.3.1 I2C Interface Timing



RESET TIMING

		FAST-MODE		
ITEM	SYMBOL	MIN.	MAX.	UNIT
SCL CLOCK FREQUENCY	f_{SCL}	0	400	kHz
HOLD TIME START CONDITION	$t_{HD:STA}$	0.6	—	us
LOW PERIOD OF THE SCL CLOCK	t_{Low}	1.3	—	us
HIGH PERIOD OF THE SCL CLOCK	t_{High}	0.6	—	us
SET-UP TIME FOR A REPEATED START CONDITION	$t_{SU:STA}$	0.6	—	us
DATA HOLD TIME	$t_{HD:DAT}$	100	—	ns
DATA SET-UP TIME	$t_{SU:DAT}$	100	—	ns
RISE TIME OF BOTH SDA AND SCL SIGNALS (30% TO 70%)	tr	—	300	ns
FALL TIME OF BOTH SDA AND SCL SIGNALS (70% TO 30%)	tf	—	300	ns
SIGNAL PULSE GLITCH TOLERANCE	t_{SP}	—	50	ns
SET-UP TIME FOR STOP CONDITION	$t_{SU:STO}$	0.6	—	us
BUS FREE TIME BETWEEN A STOP AND START CONDITION	t_{BUF}	1.3	—	us

5.4 POWER ON/OFF SEQUENCE



TIMING RELATION OF POWER ON/OFF SEQUENCE

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT
T_{Rise1}	IOVCC RISE TIME	0.05	—	20	ms
T_{Rise2}	AVDD/AVEE RISE TIME	0.05	—	20	ms
T_{Fall}	EXTERNAL POWER FALL TIME	0.05	—	20	ms
T_{B-A}	DELAY TIME BETWEEN TWO EXTERNAL POWER	2	5	—	ms
T_{Reset}	DELAY TIME BETWEEN EXTERNAL POWER AND RESET	4	10	—	ms
$T_{Reset-CMD}$	RESET TO FIRST COMMAND IN DISPLAY SLEEP IN MODE	10	—	—	ms
V_{init}	INITIALIZE VOLTAGE			100	mV

NOTE(1) : BEFORE VDDI POWER ON, PLEASE MAKE SURE VDDI, VDD, VDD_TP ARE UNDER 100mV FOR 10ms.

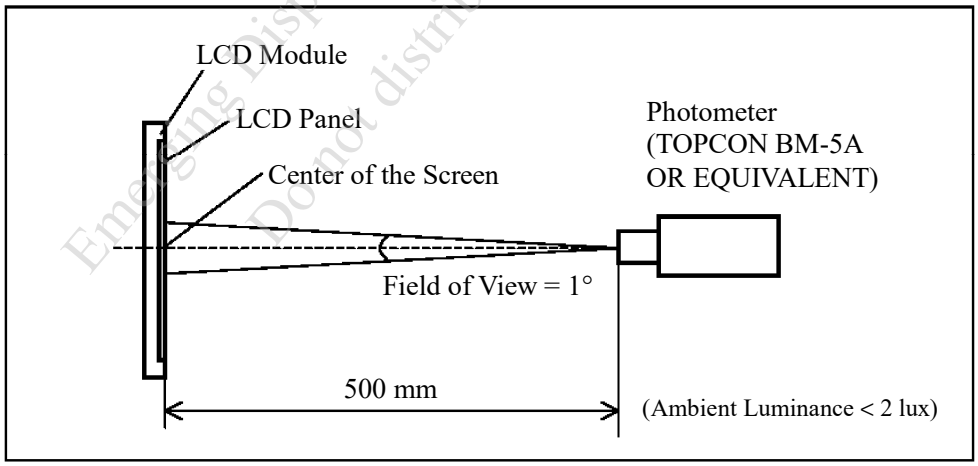
6. OPTICAL CHARACTERISTICS (NOTE 1)

6.1 OPTICAL CHARACTERISTICS

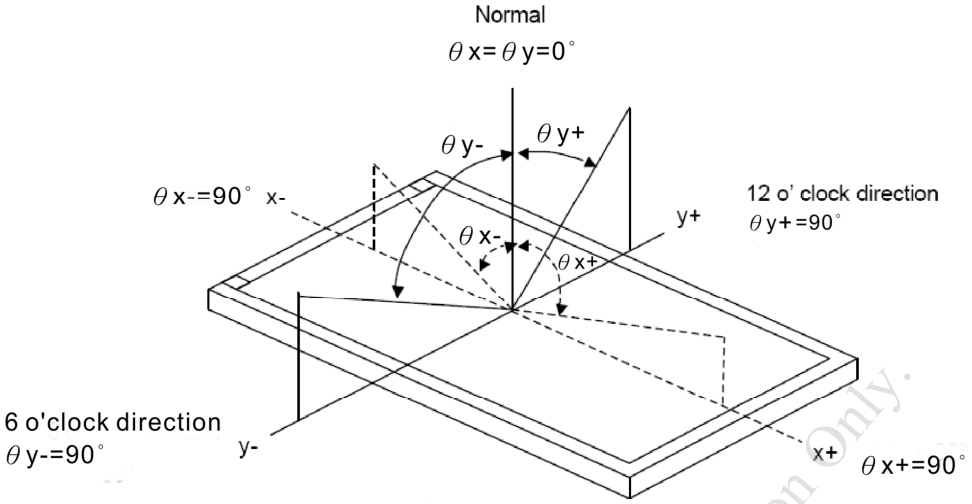
Ta=25±2°C

ITEM		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE		θ_{y+}	CR ≥ 10	θ_x=0°	(75)	(80)	—	deg.	NOTE (2) NOTE (3)
		θ_{y-}			(75)	(80)	—		
		θ_{x+}		θ_y=0°	(75)	(80)	—		
		θ_{x-}			(75)	(80)	—		
CONTRAST RATIO(CENTER)		CR	θx=0° , θy=0°		(1200)	—	—	—	NOTE (3)
RESPONSE TIME		Tr + Tf			—	25	30	msec	NOTE (4)
COLOR CHROMATICITY (CENTER)	WHITE	Wx	θx=0° , θy=0° ILED=600mA NTSC : (64.7%)		(0.597)	(0.647)	(0.697)	—	NOTE (5)
		Wy			(0.268)	(0.318)	(0.368)		
	RED	Rx			(0.213)	(0.263)	(0.313)	—	
		RY			(0.499)	(0.549)	(0.599)		
	GREEN	Gx			(0.090)	(0.140)	(0.190)	—	
		Gy			(0.040)	(0.090)	(0.140)		
	BLUE	Bx			(0.236)	(0.286)	(0.336)	—	
		By			(0.256)	(0.306)	(0.356)		
THE BRIGHTNESS OF MODULE (CENTER)		B			(900)	(1000)	—	cd/m^2	NOTE (6)
THE UNIFORMITY OF MODULE		—			70	75	—	%	NOTE (7)

NOTE (1)：TEST CONDITION：
AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES. MEASUREMENT SHOULD BE EXECUTED IN A STABLE, WINDLESS, AND DARK ROOM.



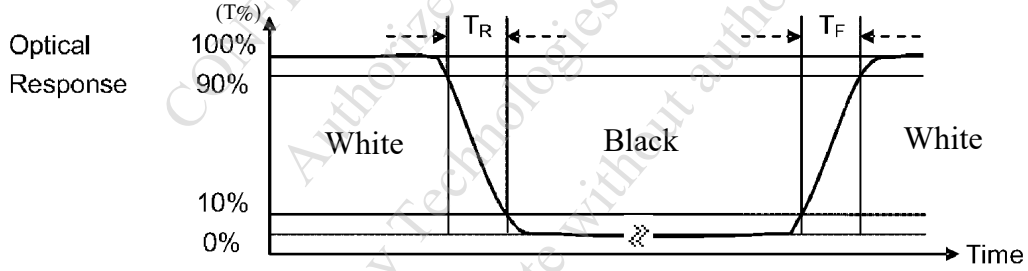
NOTE (2)：DEFINITION OF VIEWING ANGLE：



NOTE (3)：DEFINITION OF CONTRAST RATIO (CR) :
MEASURED AT THE CENTER POINT OF MODULE

$$\text{CONTRAST RATIO(CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

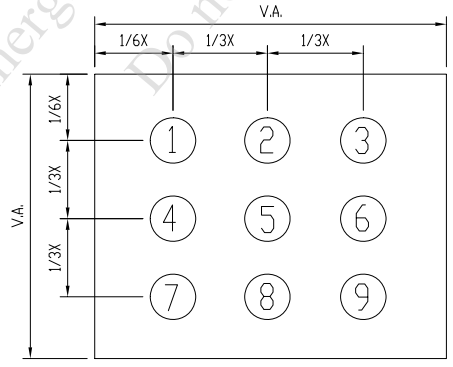
NOTE (4)：DEFINITION OF RESPONSE TIME : T_R AND T_F
THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



NOTE (5)：DEFINITION OF COLOR CHROMATICITY
(a)100% RGB PIXEL DATA TRANSMISSION WHEN ALL THE INPUT TERMINALS OF MODULE ARE ELECTRICALLY POWERED ON.
(b)MEASURED AT THE CENTER POINT OF MODULE

NOTE (6)：MEASURED THE BRIGHTNESS OF WHITE STATE AT CENTER POINT.

NOTE (7)：(a)DEFINITION OF BRIGHTNESS UNIFORMITY

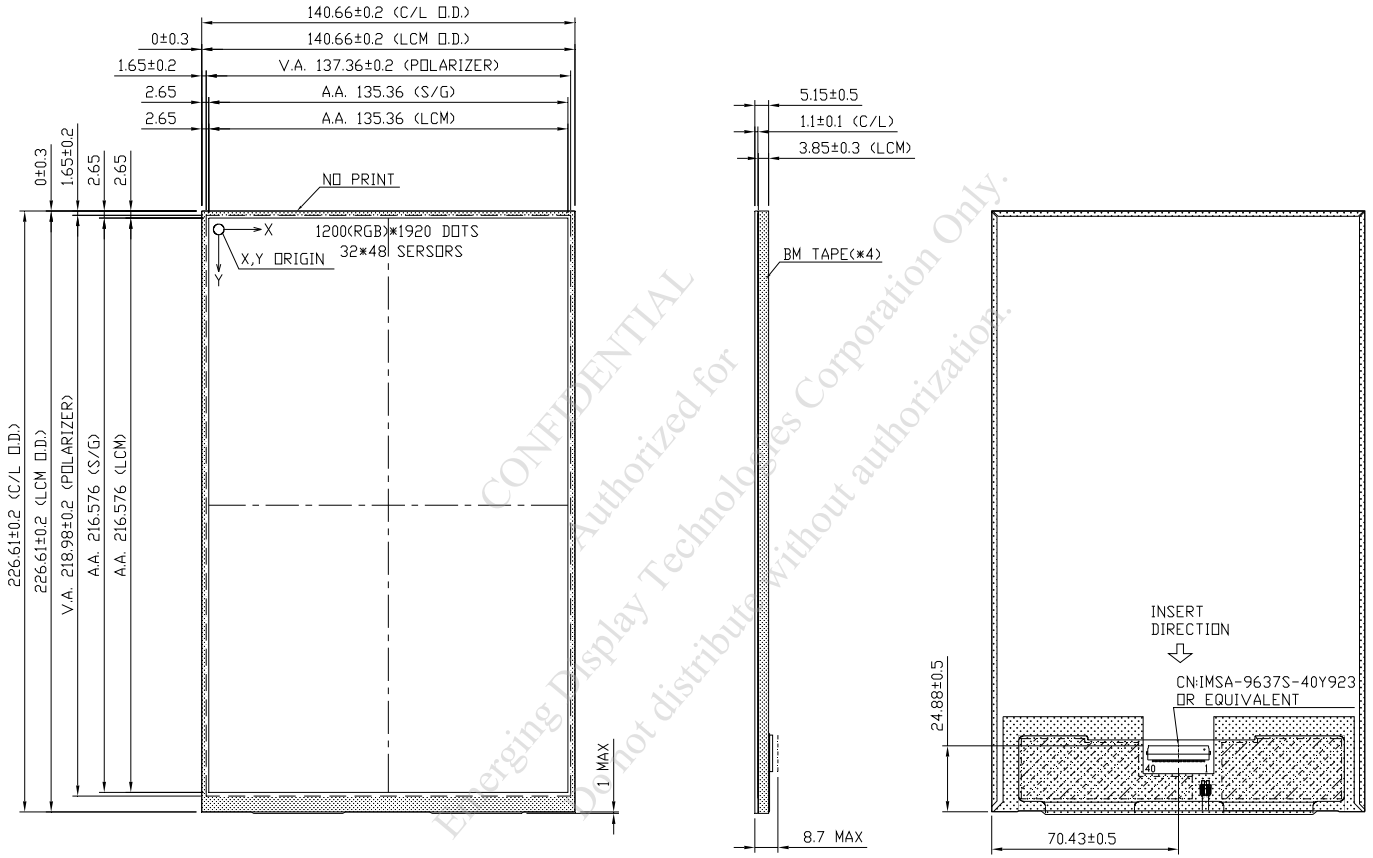


UNIT：mm

(b)THE BRIGHTNESS UNIFORMITY CALCULATING METHOD

$$\text{UNIFORMITY}：\frac{\text{MINIMUM BRIGHTNESS}}{\text{MAXIMUM BRIGHTNESS}} *100\%$$

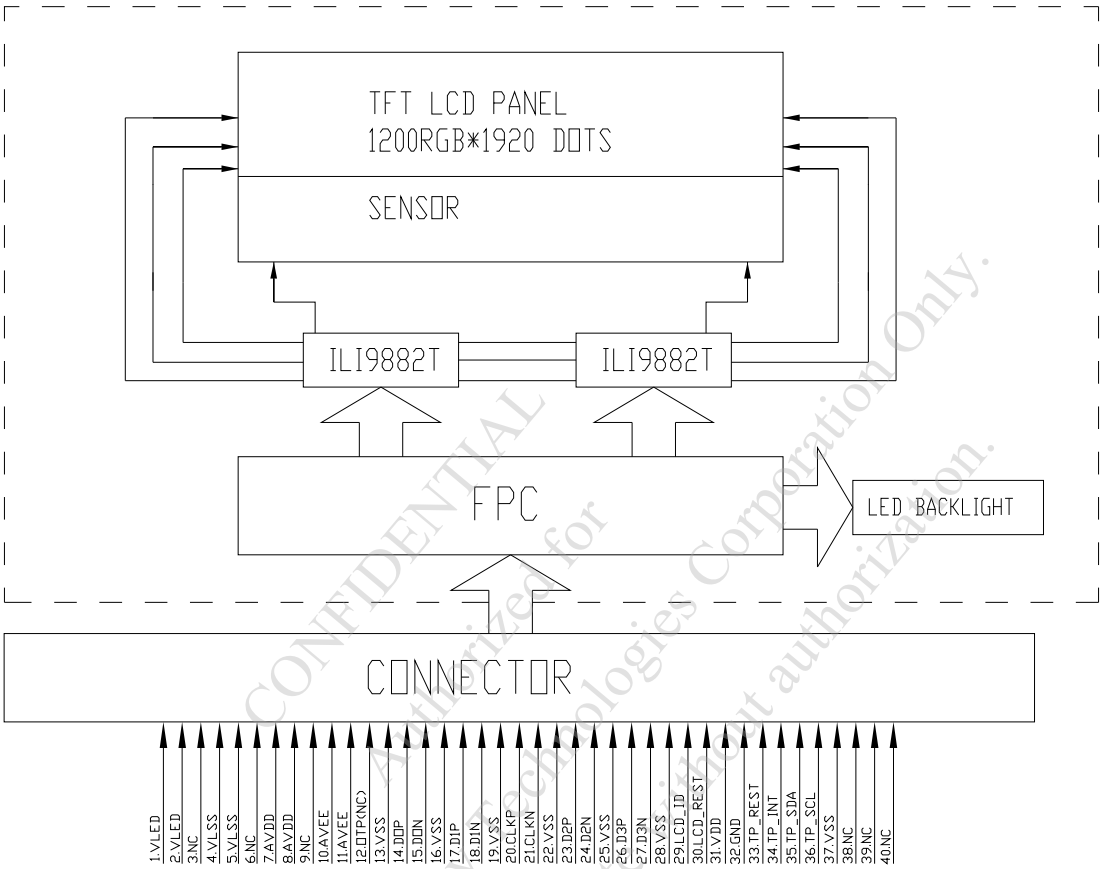
7. OUTLINE DIMENSIONS



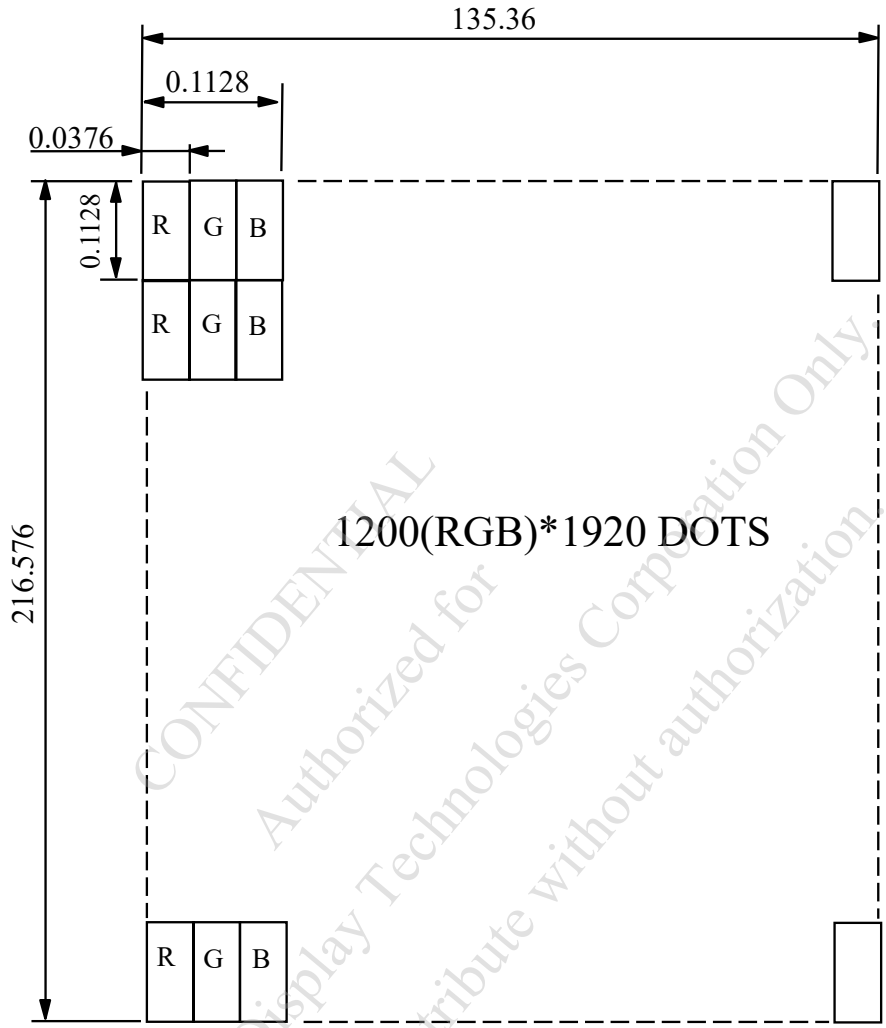
UNIT : mm
SCALE : NTS
THIRD ANGLE PROJECTION
NOT SPECIFIED TOLERANCE IS ± 0.5
NOTE :
1. C/L GLASS : SODA-LIME, NON-STRENGTHEN, CHAMFERED EDGES.

8. BLOCK DIAGRAM

8.1 TFT AND CTP MODULE



9. DETAIL DRAWING OF DOT MATRIX



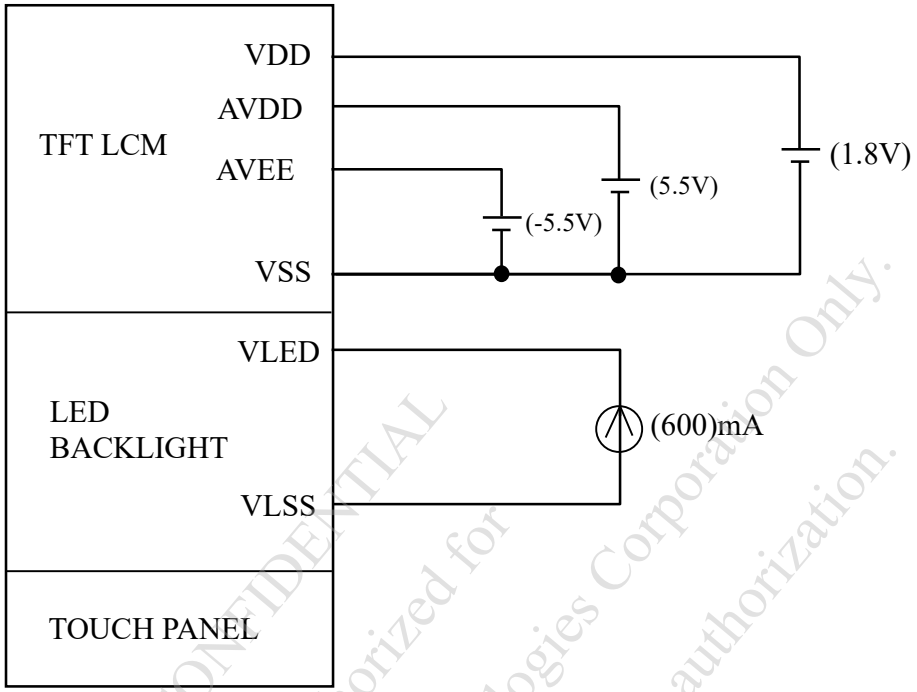
UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.1
DOTS MATRIX TOLERANCE IS ± 0.01

10. INTERFACE SIGNALS

PIN NO.	SYMBOL	FUNCTION
1	VLED	POWER FOR LED BACKLIGHT(ANODE)
2	VLED	POWER FOR LED BACKLIGHT(ANODE)
3	NC	NO CONNECTION
4	VLSS	POWER FOR LED BACKLIGHT(CATHODE)
5	VLSS	POWER FOR LED BACKLIGHT(CATHODE)
6	NC	NO CONNECTION
7	AVDD	POSITIVE INPUT POWER
8	AVDD	POSITIVE INPUT POWER
9	NC	NO CONNECTION
10	AVEE	NEGATIVE INPUT POWER
11	AVEE	NEGATIVE INPUT POWER
12	OTP(NC)	NO CONNECTION
13	VSS	GROUND
14	DOP	POSITIVE MIPI DIFFERENTIAL DATA INPUT
15	DON	NEGATIVE MIPI DIFFERENTIAL DATA INPUT
16	VSS	GROUND
17	D1P	POSITIVE MIPI DIFFERENTIAL DATA INPUT
18	D1N	NEGATIVE MIPI DIFFERENTIAL DATA INPUT
19	VSS	GROUND
20	CLKP	POSITIVE MIPI DIFFERENTIAL CLK INPUT
21	CLKN	NEGATIVE MIPI DIFFERENTIAL CLK INPUT
22	VSS	GROUND
23	D2P	POSITIVE MIPI DIFFERENTIAL DATA INPUT
24	D2N	NEGATIVE MIPI DIFFERENTIAL DATA INPUT
25	VSS	GROUND
26	D3P	POSITIVE MIPI DIFFERENTIAL DATA INPUT
27	D3N	NEGATIVE MIPI DIFFERENTIAL DATA INPUT
28	VSS	GROUND
29	LCD_ID	ID(10K TO GND)
30	LCD_REST	GLOBAL RESET PIN
31	VDD	LOGIC INPUT POWER
32	GND	GROUND
33	TP_REST	TP GLOBAL RESET PIN
34	TP_INT	TP INT PIN
35	TP_SDA	TP SDA PIN
36	TP_SCL	TP SCL PIN
37	VSS	GROUND
38	NC	NO CONNECTION
39	NC	NO CONNECTION
40	NC	NO CONNECTION

11. POWER SUPPLY

11.1 POWER SUPPLY FOR LCM



12. CAPACITIVE TOUCH PANEL SPECIFICATION

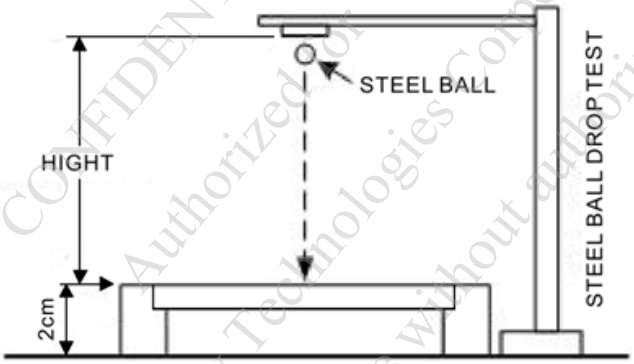
12.1 HARDNESS

ITEM	DESCRIPTION
SURFACE HARDNESS	(7)H (MIN.)

12.2 DURABILITY

USING STEEL BALL AND FALLING ON TOUCH PANEL SURFACE, FROM THE HEIGHT MUST PASS BELOW CONDITIONS：

ITEM	CONDITION	INSPECTION METHOD	DESCRIPTION
STEEL BALL DROP TEST	WEIGHT：67g HEIGHT OF FALL：30 cm	VISUAL INSPECTION	SIGN OF FRACTURE OR DAMAGE IS NOT ACCEPTABLE 3 TIME/ 1 POINTS, 25°C (CENTER POINT)



13 INSPECTION CRITERIA

13.1 APPLICATION

THIS INSPECTION STANDARD IS TO BE APPLIED TO THE LCD MODULE DELIVERED FROM EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) TO CUSTOMERS

13.2 INSPECTION CONDITIONS

13.2.1 (1)OBSERVATION DISTANCE：45±5cm

(2)VIEWING ANGLE：±45°

±45° (FOR SECTION WITHIN VIEWING AREA), REFER TO FIG.A

90° (FOR SECTION OUTSIDE OF VIEWING AREA), REF TO FIG.B

PERPENDICULAR TO MODULE SURFACE

VIEWING ANGLE SHOULD BE SMALLER THAN 45°

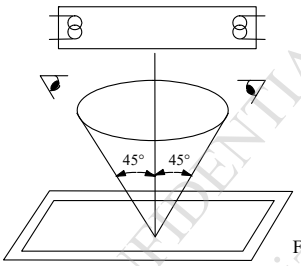


FIG.A

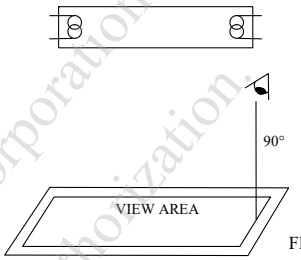


FIG.B

THE INSPECTION CRITERIA IS ACCORDING TO LINE OF SIGHT. INSPECTION SHALL BE MADE WITHIN THE HALF SECTION OF THE VIEWING CONE GENERATED BY LINE SEGMENT OF 45° WITH RESPECT TO THE VERTICAL AXIS FROM CENTER VERTEX OF LCD, THE FLUORESCENT LAMP AND THE CONE AXIS MUST BE PERPENDICULAR TO THE LCD SURFACE.

IF THE DEFECTS ARE OUTSIDE OF VIEWING AREA, IT SHALL BE INSPECTED BY 90° WITH RESPECT TO THE VERTICAL AXIS FROM EDGE OF VIEWING AREA.

13.2.2 ENVIRONMENT CONDITIONS：

AMBIENT TEMPERATURE		25±5°C
AMBIENT HUMIDITY		55 ± 20%RH
AMBIENT ILLUMINATION	COSMETIC INSPECTION	600~800 lux
	FUNCTIONAL INSPECTION	200~500 lux
INSPECTION TIME		15 secs

13.2.3 INSPECTION LOT

QUANTITY PER DELIVERY LOT FOR EACH MODEL

13.2.4 INSPECTION METHOD

A SAMPLING INSPECTION SHALL BE MADE ACCORDING TO THE FOLLOWING PROVISIONS TO JUDGE THE ACCEPTABILITY

(a)APPLICABLE STANDARD：

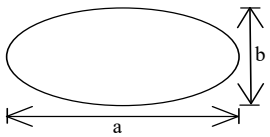
ANSI/ ASQ Z1.4 NORMAL INSPECTION LEVEL II

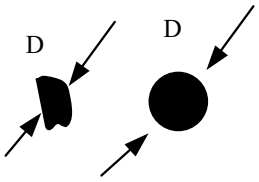
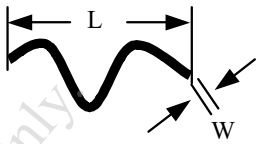
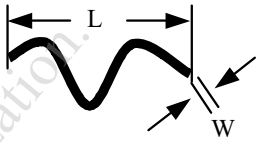
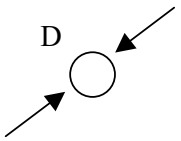
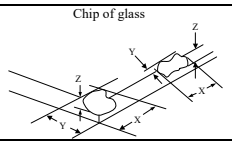
(b)AQL : MAJOR DEFECT：AQL 0.65

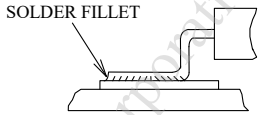
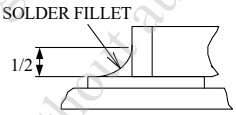
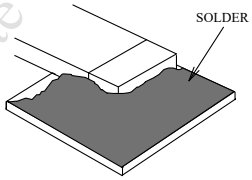
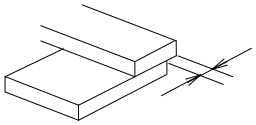
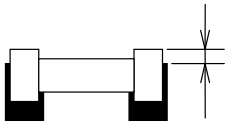
MINOR DEFECT：AQL 1.0

13.3 DEFECTS CLASSIFICATION

TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	• DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS EX: DISCONNECTION, SHORT CIRCUIT ETC	0.65
	2.CTP FUNCTION	• NO FUNCTION • BROKEN LINE • FALSE TOUCH	
	3.BACKLIGHT	• NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION	
	4.DIMENSIONS	• SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS	
MINOR DEFECT	1.DISPLAY ZONE	• BLACK/WHITE SPOT • BUBBLES ON POLARIZER • NEWTON RING • BLACK/WHITE LINE • SCRATCH • CONTAMINATION • UNEVEN COLOR SPREAD	1.0
	2.BEZEL ZONE	• STAINS • SCRATCHES • FOREIGN MATTER	
	3.SOLDERING	• INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS	
	4.DISPLAY ON (ALL ON)	• LIGHT LINE	

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th></tr>
<tr><td>1</td><td>DISPLAY ON INSPECTION</td><td>1.INCORRECT PATTERN
2.MISSING SEGMENT
3.DIM SEGMENT
4.OPERATING VOLTAGE BEYOND SPEC</td></tr>
<tr><td>2</td><td>OVERALL DIMENSIONS</td><td>1.OVERALL DIMENSION BEYOND SPEC</td></tr>
<tr><td>3</td><td>DOT DEFECT</td><td>(1)INSPECTION PATTERN: FULL WHITE, FULL BLACK, RED, GREEN AND BLUE SCREENS.
(2)
<table>
<tr><th>DEFECT TYPE</th><th>CRITERIA</th></tr>
<tr><td>BRIGHT DOT</td><td>N ≤ 3</td></tr>
<tr><td>DARK DOT</td><td>N ≤ 4</td></tr>
<tr><td>TOTAL BRIGHT AND DARK DOT</td><td>N ≤ 6</td></tr>
</table>
NOTE：
1. DEFINITION OF DOT DEFECT INDUCED FROM THE PANEL INSIDE
(A) BRIGHT DOT：DOTS APPEAR BRIGHT AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER BLACK PATTERN.
(B) DARK DOT：DOTS APPEAR DARK AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER PURE RED, GREEN, BLUE PICTURE.
(C) 2 DOT ADJACENT = 1 PAIR = 2 DOTS
PICTURE:
 
2 dot adjacent　2 dot adjacent (vertical)　2 dot adjacent (slant)</td></tr>
<tr><td>4</td><td>BUBBLES OF POLARIZER /DIRT/CF FAIL /SURFACE STAINS</td><td>
<table>
<tr><th></th><th>AVERAGE DIAMETER (mm)：D</th><th>NUMBER OF PIECES PERMITTED</th></tr>
<tr><td rowspan="3">BUBBLE ON THE POLARIZER</td><td>D ≤ 0.3</td><td>IGNORE</td></tr>
<tr><td>0.3 < D ≤ 0.5</td><td>N ≤ 4</td></tr>
<tr><td>0.5 < D</td><td>NONE</td></tr>
<tr><td rowspan="3">SURFACE STAINS</td><td>D ≤ 0.3</td><td>IGNORE</td></tr>
<tr><td>0.3 < D ≤ 0.5</td><td>N ≤ 4</td></tr>
<tr><td>0.5 < D</td><td>NONE</td></tr>
<tr><td rowspan="3">CF FAIL / SPOT</td><td>D ≤ 0.3</td><td>IGNORE</td></tr>
<tr><td>0.3 < D ≤ 0.5</td><td>N ≤ 4</td></tr>
<tr><td>0.5 < D</td><td>NONE</td></tr>
</table>
NOTE : (1)POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA.
(2)THE EXTRANEOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON.
(3)THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING.
AVERAGE DIAMETER (D)=(a+b)/2
 
</td></tr>
</table>

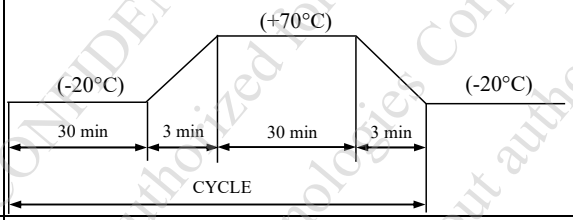
<table>
<tr><th>NO.</th><th>ITEM</th><th colspan="2">CRITERIA</th></tr>
<tr><td>5</td><td>BLACK/WHITE SPOT CIRCULAR TYPE</td><td>THE FOLLOWING BLACK/WHITE SPOT ARE WITHIN THE VIEWING AREA. AVERAGE DIAMETER：D (mm)
<table><tr><th>SIZE D</th><th>PERMISSIBLE NO.</th></tr><tr><td>D≤0.3</td><td>IGNORE</td></tr><tr><td>0.3<D≤0.5</td><td>6</td></tr><tr><td>D>0.5</td><td>0</td></tr></table>NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td><td>  </td></tr>
<tr><td>6</td><td>SCRATCH</td><td>THE FOLLOWING SCRATCH IS WITHIN THE VIEWING AREA. WIDTH：W (mm) , LENGTH : L (mm)
<table><tr><th>SIZE W & L</th><th>PERMISSIBLE NO.</th></tr><tr><td>W≤0.07</td><td>IGNORE</td></tr><tr><td>0.07<W≤0.1, L≤10</td><td>6</td></tr><tr><td>W>0.1</td><td>0</td></tr></table>NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td><td>  </td></tr>
<tr><td>7</td><td>BLACK / WHITE LINE LINEAR TYPE / FOREIGN FIBER</td><td>THE FOLLOWING BLACK LINE, WHITE LINE IS WITHIN THE VIEWING AREA. WIDTH：W (mm) , LENGTH : L (mm)
<table><tr><th>SIZE W & L</th><th>PERMISSIBLE NO.</th></tr><tr><td>W≤0.07</td><td>IGNORE</td></tr><tr><td>0.07<W≤0.1, L≤10</td><td>6</td></tr><tr><td>W>0.1</td><td>0</td></tr></table>NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td><td>  </td></tr>
<tr><td>8</td><td>BUBBLE / DENT FOR OPTICAL BONDING</td><td>BUBBLES WITHIN VIEWING AREA.
AVERAGE DIAMETER：D (mm)
<table><tr><th>SIZE D</th><th>PERMISSIBLE NO.</th></tr><tr><td>D≤0.3</td><td>IGNORE</td></tr><tr><td>0.3<D≤0.5</td><td>6</td></tr><tr><td>D>0.5</td><td>0</td></tr></table>NOTE (1)：THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.</td><td>  </td></tr>
<tr><td>9</td><td>CHIPPING</td><td><table><tr><td>CORNER</td><td>X ≤ 3mm、Y ≤ 3mm、Z ≤ t
(t : THICKNESS)</td></tr><tr><td>EDGE</td><td>X ≤ 6mm , Y ≤ 1mm , Z < t
(t : THICKNESS)</td></tr></table></td><td>  </td></tr>
<tr><td>10</td><td>CRACKED GLASS</td><td colspan="2">NOT ACCEPTABLE</td></tr>
<tr><td>11</td><td>LINE DEFECT ON DISPLAY</td><td colspan="2">OBVIOUS VERTICAL OR HORIZONTAL LINE DEFECT IS NOT ALLOWED.</td></tr>
<tr><td>12</td><td>MURA & LEAK ON DISPLAY</td><td colspan="2">IT'S ACCEPTABLE, IF MURA AND LEAK IS SLIGHT VISIBLE THROUGH 6% ND FILTER.</td></tr>
<tr><td>13</td><td>UNEVEN COLOR SPREAD, COLORATION</td><td colspan="2">TO BE DETERMINED BASED UPON THE LIMITED SAMPLE.</td></tr>
<tr><td>14</td><td>BEZEL APPEARANCE</td><td colspan="2">1. BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS OF OTHER CONTAMINATION.
2. BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.</td></tr>
<tr><td>15</td><td>MURA</td><td colspan="2">NOT VISIBLE THROUGH 6% ND FILTER IN 50% GRAY.</td></tr>
</table>

NO.	ITEM	CRITERIA
16	PCB	1. THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES. 2. NO OXIDATION OR CONTAMINATION ON PCB TERMINALS. 3. PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART. THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS. 4. THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART. 5. IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD; MAKE SURE IT IS SMOOTHED DOWN.
17	SOLDERING	1. NO SOLDERING FOUND ON THE SPECIFIED PLACE 2. INSUFFICIENT SOLDER (a)LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR "HEEL" OF LEAD AND PAD  (b)CHIP COMPONENT · SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING  · SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  3. PARTS ALIGNMENT (a)LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE  (b)CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  4. NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. 5. NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. 6. NO RESIDUE OR SOLDER BALLS ON PCB. 7. NO SHORT CIRCUITS IN COMPONENTS ON PCB.

NO.	ITEM	CRITERIA
18	BACKLIGHT	1. NO LIGHT 2. FLICKERING AND OTHER ABNORMAL ILLUMINATION 3. SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. 4. BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.
19	GENERAL APPEARANCE	1. NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. 2. NO CRACKS ON INTERFACE PIN (OLB) OF TCP. 3. NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. 4. THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. 5. THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. 6. THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. 7. SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. 8. PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. 9. LCD PIN LOOSE OR MISSING PINS. 10. PRODUCT PACKAGING MUST BE THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. 11. PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. 12. THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

14 RELIABILITY TEST

14.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO.	ITEM	DESCRIPTION
1	HIGH TEMPERATURE TEST (OPERATION)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT (+70°C) FOR 240 HRS
2	LOW TEMPERATURE TEST (OPERATION)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT (-20°C) FOR 240 HRS
3	HIGH TEMPERATURE TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT (+70°C) FOR 240 HRS
4	LOW TEMPERATURE TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT (-20°C) FOR 240 HRS
5	HIGH TEMPERATURE / HUMIDITY TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT 60°C, 90% RH 240 HRS
6	THERMAL SHOCK TEST (NOT OPERATED)	THE SAMPLE SHOULD BE ALLOWED TO STAND THE FOLLOWING 10 CYCLES OF OPERATION： 
7	ESD (ELECTROSTATIC DISCHARGE) (NOT OPERATED)	AIR DISCHARGE ± 12KV CONTACT DISCHARGE ± 8KV (ACCORDING TO IEC-61000-4-2)

NOTE (1)：THE TEST SAMPLES HAVE RECOVERY TIME FOR 2 HOURS AT ROOM TEMPERATURE BEFORE THE FUNCTION CHECK. IN THE STANDARD CONDITIONS, THERE IS NO DISPLAY FUNCTION NG ISSUE OCCURRED.

NOTE (2)：WHEN THE LCD MODULE IS OPERATED AT A HIGHER AMBIENT TEMPERATURE THAN 60°C, THE PWM DUTY CYCLE OF THE LED BACKLIGHT SHOULD BE ADJUSTED TO BE LESS THAN TBD%. IF THE MODULE IS OPERATED AT A HIGHER DUTY CYCLE THAN TBD, THEN THERE IS A POSSIBILITY OF DISTORTION AND IRREGULARITY OF THE PICTURE DUE TO LIQUID CRYSTAL BEHAVIOR.

NOTE (3)：TESTING CONDITIONS AND INSPECTION CRITERIA

NO.	ITEM	TEST MODEL	INSPECTION CRITERIA
1	CURRENT CONSUMPTION	REFER TO SPECIFICATION	THE CURRENT CONSUMPTION SHOULD CONFORM TO THE PRODUCT SPECIFICATION.
2	CONTRAST	REFER TO SPECIFICATION	AFTER THE TESTS HAVE BEEN EXECUTED, THE CONTRAST MUST BE LARGER THAN HALF OF ITS INITIAL VALUE PRIOR TO THE TESTS.
3	APPEARANCE	VISUAL INSPECTION	DEFECT FREE

15. CAUTION

15.1 OPERATION

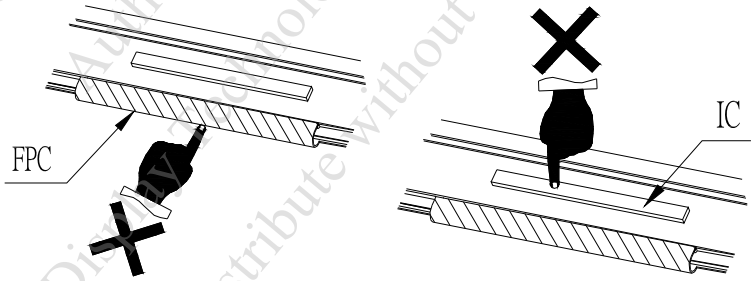
15.1.1 DO NOT CONNECT OR DISCONNECT MODULES TO OR FROM THEMAIN SYSTEM WHILE POWER IS BEING SUPPLIED .

15.1.2 USE THE MODULE WITHIN SPECIFIED TEMPERATURE ; LOWER TEMPERATURE CAUSES THE RETARDATION OF BLINKING SPEED OF THE DISPLAY ; HIGHER TEMPERATURE MAKES OVERALL DISPLAY DISCOLOR.
WHEN THE TEMPERATURE RETURNS TO NORMALITY, THE DISPLAY WILL OPERATE NORMALLY .

15.1.3 ADJUST THE LC DRIVING VOLTAGE TO OBTAIN THE OPTIMUM CONTRAST.

15.1.4 POWER ON SEQUENCE INPUT SIGNALS SHOULD NOT BE SUPPLIED TO LCD MODULE BEFORE POWER SUPPLY VOLTAGE IS APPLIED AND REACHES THE SPECIFIED VALUE .
IF ABOVE SEQUENCE IS NOT FOLLOWED , CMOS LSIS OF LCD MODULES MAY BE DAMAGED DUE TO LATCH - UP PROBLEM .

15.1.5 NOT ALLOWED TO INFLICT ANY EXTERNAL STRESS AND TO CAUSE ANY MECHANICAL INTERFERENCE ON THE BENDING AREA OF FPC DURING THE TAIL BENDING BACKWARDS!
DO NOT STRESS FPC AND IC ON THE MODULE!



15.2 NOTICE

15.2.1 USE A GROUNDED SOLDERING IRON WHEN SOLDERING CONNECTOR I/O TERMINALS . FOR SOLDERING OR REPAIRING, TAKE PRECAUTION AGAINST THE TEMPERATURE OF THE SOLDERING IRON AND THE SOLDERING TIME TO PREVENT PEELING OFF THE THROUGH-HOLE-PAD .

15.2.2 DO NOT DISASSEMBLE . EDT SHALL NOT BE HELD RESPONSIBLE IF THE MODULE IS DISASSEMBLED AND UPON THE REASSEMBLY THE MODULE FAILED .

15.2.3 DO NOT CHARGE STATIC ELECTRICITY , AS THE CIRCUIT OF THIS MODULE CONTAINS CMOS LSIS. A WORKMAN'S BODY SHOULD ALWAYS BE STATIC-PROTECTED BY USE OF AN ESD STRAP. WORKING CLOTHES FOR SUCH PERSONNEL SHOULD BE OF STATIC-PROTECTED MATERIAL.

15.2.4 ALWAYS GROUND THE ELECTRICALLY-POWERED DRIVER BEFORE USING IT TO INSTALL THE LCD MODULE. WHILE CLEANING THE WORK STATION BY VACUUM CLEANER, DO NOT BRING THE SUCKING MOUTH NEAR THE MODULE ; STATIC ELECTRICITY OF THE ELECTRICALLY-POWERED DRIVER OR THE VACUUM CLEANER MAY DESTROY THE MODULE .

15.2.5 DON'T GIVE EXTERNAL SHOCK.

15.2.6 DON'T APPLY EXCESSIVE FORCE ON THE SURFACE.

15.2.7 LIQUID IN LCD IS HAZARDOUS SUBSTANCE. MUST NOT LICK AND SWALLOW.
WHEN THE LIQUID IS ATTACH TO YOUR, SKIN, CLOTH ETC.
WASH IT OUT THOROUGHLY AND IMMEDIATELY.

15.2.8 DON'T OPERATE IT ABOVE THE ABSOLUTE MAXIMUM RATING.

15.2.9 STORAGE IN A CLEAN ENVIRONMENT, FREE FROM DUST, ACTIVE GAS AND SOLVENT.

15.2.10 STORE WITHOUT ANY PHYSICAL LOAD.

15.2.11 REWIRING: NO MORE THAN 3 TIMES.