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Vincent Wh		VERSION : 2

CUSTOMER ACCEPTANCE SPECIFICATIONS

MODEL NO. :
EIML070022DYA
 (RoHS)
 FOR MESSRS :

CUSTOMER'S APPROVAL

DATE :

BY :

RECORDS OF REVISION

MAY.21, 2024

DATE

REVISED
PAGE
NO.

SUMMARY

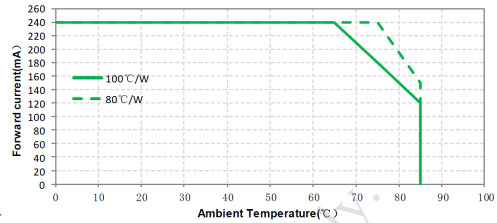
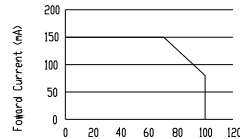
MAY.29, 2024

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4. ELECTRICAL CHARACTERISTICS

NOTE(3):

Ambient Temperature VS Maximum Forward Current



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1. GENERAL SPECIFICATIONS

1.1 DATA SHEETS FOR CONTROLLER / DRIVER PLEASE REFER TO :

FOCAL FT8206

1.2 MATERIAL SAFETY DESCRIPTION

ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED DIPHENYL ETHERS (PBDE), BIS(2-ETHYLHEXYL) PHTHALATE (DEHP), BUTYL BENZYL PHTHALATE (BBP), DIBUTYL PHTHALATE (DBP), DIISOBUTYL PHTHALATE (DIBP).

2. MECHANICAL SPECIFICATIONS

2.1 TFT LCD MODULE MECHANICAL SPECIFICATIONS

(1) DISPLAY SIZE	-----	7 inch
(2) NUMBER OF DOTS	-----	1200(RGB)W * 1920H DOTS
(3) MODULE SIZE	-----	106.5W * 163.2H * 5.25D mm (WITHOUT FPC)
(4) VIEWING AREA	-----	95.3W * 152.0H mm
(5) ACTIVE AREA	-----	94.5W * 151.2H mm
(6) DOT SIZE	-----	0.02625W * 0.07875H mm
(7) PIXEL SIZE	-----	0.07875W * 0.07875H mm
(8) LCD TYPE	-----	TFT, IPS, TRANSMISSIVE, ANTI-GLARE
(9) COLOR	-----	16.7M
(10) VIEWING DIRECTION	-----	SUPER WIDE VIEW
(11) BACK LIGHT	-----	LED , COLOR : WHITE
(12) INTERFACE MODE	-----	MIPI
(13) WEIGHT	-----	168g

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2.2 CAPACITIVE TOUCH PANEL MECHANICAL SPECIFICATIONS

- (1) TOUCH PANEL SIZE ----- 7 inch
- (2) OUTER DIMENSION ----- 106W * 163.23H mm * 5.25D mm
(WITHOUT FPC)
- (3) ACTIVE AREA ----- 94.5W * 151.2H mm
- (4) INPUT TYPE ----- MULTI TOUCH
- (5) NUMBER OF TOUCH SENSOR ----- 20*30 SENSORS
- (6) RESOLUTION ----- 1200 * 1920
- (7) INTERFACE MODE ----- I2C
- (8) THE MATERIAL OF COVER LENS ----- GLASS

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3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE	VDD-VSS	-0.3	1.95	V	—
	AVDD-VSS	-0.3	6.5	V	—
	AVEE-VSS	-6.5	0.3	V	—
POWER DISSIPATION FOR LED DRIVER	VLED-VLSS	-0.3	27	V	—
STATIC ELECTRICITY	—	—	—	V	NOTE (1)

NOTE (1) : LCM SHOULD BE GROUND DURING LCM HANDLING.

NOTE (2) : THE ABSOLUTE MAXIMUM RATING VALUES OF THIS PRODUCT ARE NOT ALLOWED TO BE EXCEEDED AT ANY TIMES. SHOULD A MODULE BE USED WITH ANY OF THE ABSOLUTE MAXIMUM RATINGS EXCEEDED, THE CHARACTERISTICS OF THE MODULE MAY NOT BE RECOVERED, OR IN AN EXTREME CASE, THE MODULE MAY BE PERMANENTLY DESTROYED.

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

ITEM	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20°C	70°C	-30°C	80°C	NOTE (1),(2),(3),(4)
HUMIDITY	NOTE (3)		NOTE (3)		WITHOUT CONDENSATION
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (1) : THE ABSOLUTE MAXIMUM RATINGS OF THIS PRODUCT SHOULD NOT BE EXCEEDED AT ANY TIME. IF THESE RATINGS ARE EXCEEDED, THE PRODUCT'S PERFORMANCE IS NOT GUARANTEED AND THE PRODUCT MAY EXPERIENCE PERMANENT DAMAGE.

NOTE (2) : BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (3) : $T_a \leq 60^\circ\text{C}$: 90% RH MAX.

$T_a > 60^\circ\text{C}$: ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90% RH AT 90°C .

NOTE (4) : WHEN THE LCD MODULE IS OPERATED AT A HIGHER AMBIENT TEMPERATURE THAN 60°C , THE PWM DUTY CYCLE OF THE LED BACKLIGHT SHOULD BE ADJUSTED TO BE LESS THAN TBD%. IF THE MODULE IS OPERATED AT A HIGHER DUTY CYCLE THAN TBD, THEN THERE IS A POSSIBILITY OF DISTORTION AND IRREGULARITY OF THE PICTURE DUE TO LIQUID CRYSTAL BEHAVIOR.

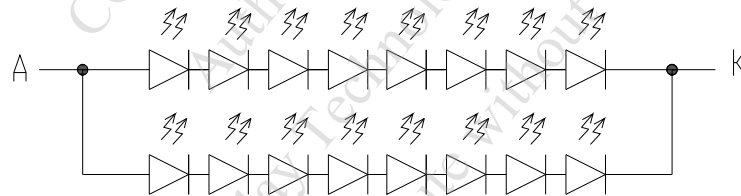
4. ELECTRICAL CHARACTERISTICS

Ta = 25 °C

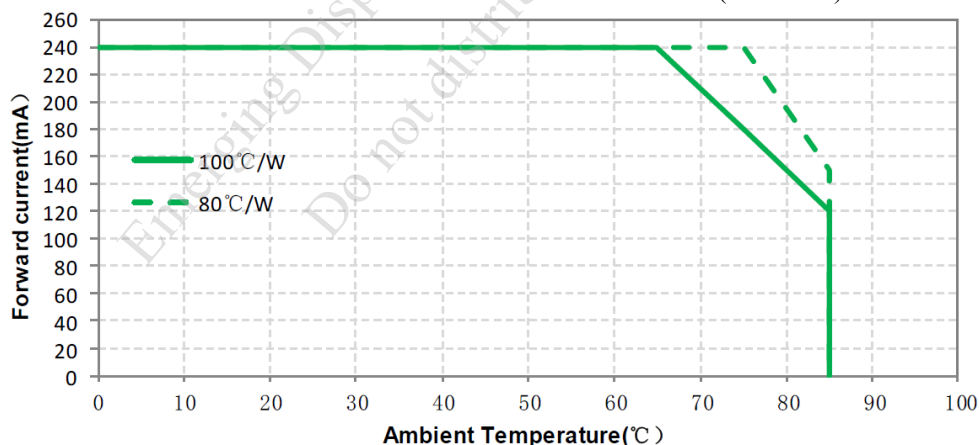
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
POWER SUPPLY VOLTAGE	VDD-VSS	—	1.65	1.80	1.95	V	
POWER SUPPLY VOLTAGE FOR CIRCUITS	AVDD-VSS	—	4.5	5.0	5.5	V	
	AVEE-VSS	—	-5.5	-5.0	-4.5	V	
POWER SUPPLY VOLTAGE FOR LED DRIVER	VLED-VLSS	—	10.8	12.0	13.2	V	
POWER SUPPLY CURRENT	IDD	VDD-VSS=1.80V	—	32	50	mA	NOTE (1)
POWER SUPPLY CURRENT FOR CIRCUITS	IAVDD	AVDD-VSS=5.0V	—	7.5	12	mA	
	IAVEE	AVEE-VSS=-5.0V	—	7.5	12		
POWER SUPPLY CURRENT FOR LED DRIVER	IVLED	VLED-VLSS=12.0V LED B/L=ON	—	370	650	mA	
POWER SUPPLY VOLTAGE FOR LED DRIVER	B/L_EN	VIH	2.5	—	—	V	
		VIL	—	—	0.8	V	
	B/L_PWM	VIH	2.5	—	—	V	
		VIL	—	—	0.8	V	
LED LIFE TIME	—	I _{LED} =80mA (PER LED)	30K	—	—	HRS	NOTE (4) NOTE (5)

NOTE (1) : THE DISPLAY PATTERN IS ALL “WHITE”.

NOTE (2) : INTERNAL CIRCUIT DIAGRAM OF BACKLIGHT



NOTE (3) : AMBIENT TEMP. VS. ALLOWABLE FORWARD CURRENT.(PER LED)



NOTE (4) : CONDITIONS; Ta=25 °C, CONTINUOUS LIGHTING.

NOTE (5) : DEFINITIONS OF LIFE TIME

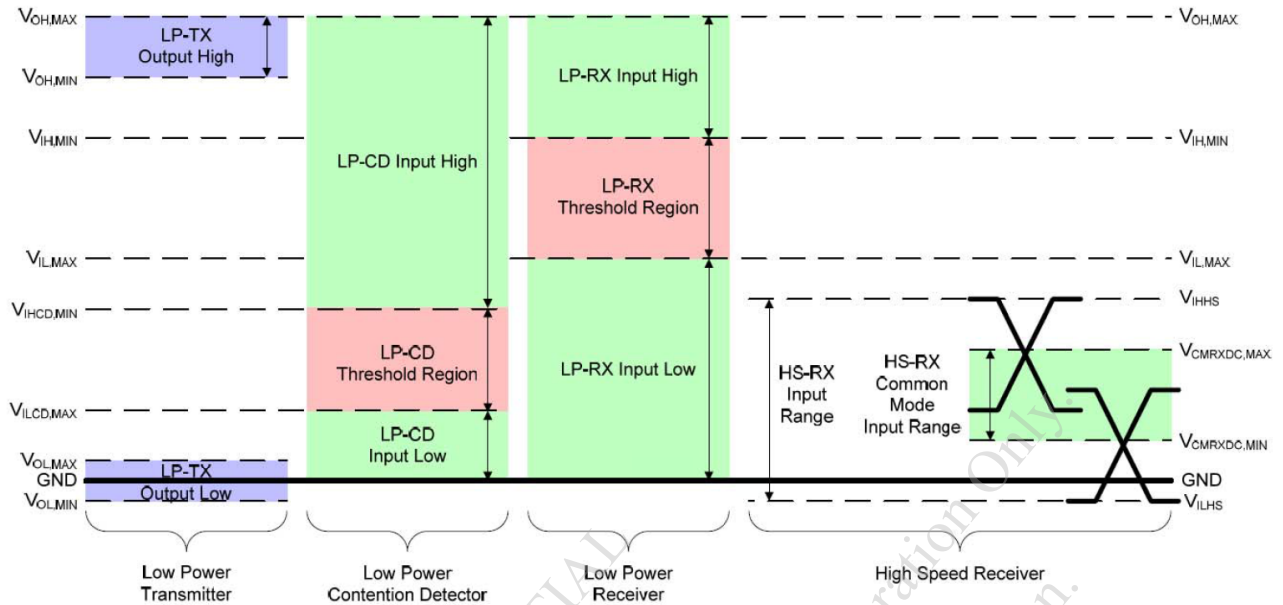
LCD LUMINANCE BECOMES HALF OF THE INITIAL VALUE.

5. TIMING CHARACTERISTICS

5.1 FOR LCD MODULE

5.1.1 MIPI D-PHY DC CHARACTER

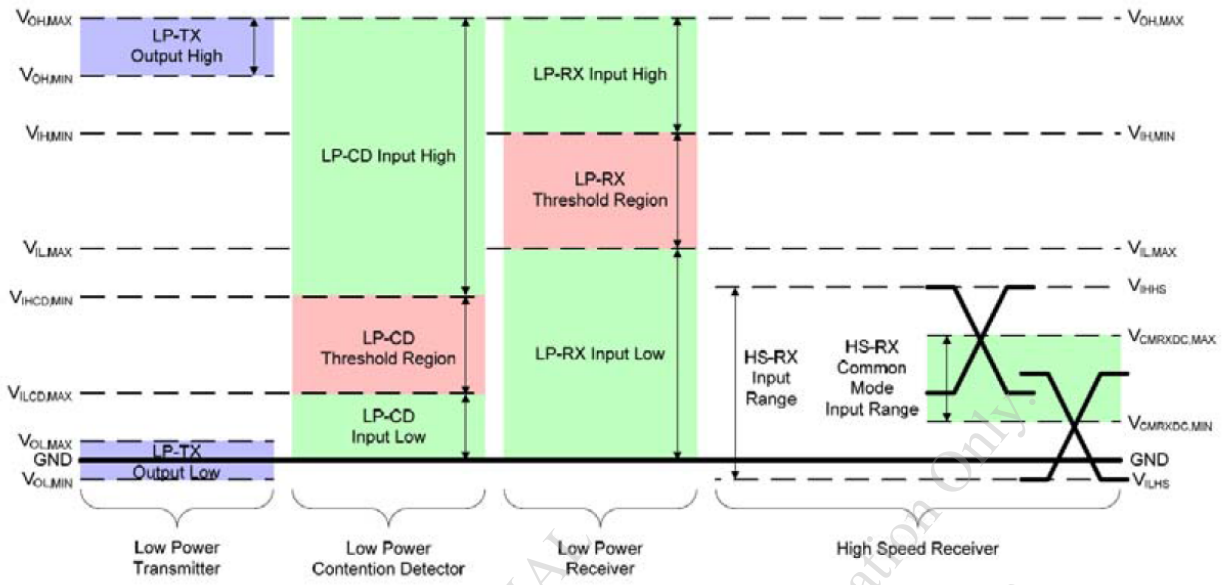
ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY VOLTAGE FOR MIPI INTERFACE						
POWER SUPPLY VOLTAGE FOR MIPI INTERFACE	LVDSVDD	—	1.08	1.3	1.35	V
LPDT INPUT CHARACTERISTICS						
PAD SIGNAL VOLTAGE RANGE	VI	—	-50	—	1350	mV
GROUND SHIFT	VGND _{SH}	—	-50	—	50	mV
LOGIC 0 INPUT THRESHOLD	VIL	—	—	—	550	mV
LOGIC 1 INPUT THRESHOLD (D-PHY SPEC)	VIH	—	880	—	—	mV
LOGIC 1 INPUT THRESHOLD (C-PHY SPEC)	VIH	—	740	—	—	mV
INPUT HYSTERESIS	VHYST	—	25	—	—	mV
LPDT OUTPUT CHARACTERISTICS						
OUTPUT LOW LEVEL	VOL	—	-50	—	50	mV
OUTPUT HIGH LEVEL (D-PHY SPEC)	VOH	—	1.1	1.2	1.3	V
OUTPUT HIGH LEVEL (C-PHY SPEC)	VOH	—	0.95	1.2	1.3	V
LOGIC 0 CONTENTION THRESHOLD	VILCD, MAX	—	—	—	200	mV
LOGIC 1 CONTENTION THRESHOLD	VIHCD, MIN	—	450	—	—	mV
OUTPUT IMPEDENCE OF LPDT	ZOLP	—	110	—	—	Ω
HI-SPEED INPUT/OUTPUT CHARACTERISTICS (D-PHY)						
SINGLE-END INPUT LOW VOLTAGE	VILHS	—	-40	—	—	mV
SINGLE-END INPUT HIGH VOLTAGE	VIHHS	—	—	—	460	mV
SINGLE-END THRESHOLD FOR HS TERMINATION ENABLE	VTERM-EN	—	—	—	450	mV
DIFFERENTIAL INPUT LOW THRESHOLD	VIDTL	—	-70	—	—	mV
DIFFERENTIAL INPUT HIGH THRESHOLD	VIDTH	—	—	—	70	mV
COMMON MODE VOLTAGE	VCMRXDC	—	70	—	330	mV
DIFFERENTIAL INPUT IMPEDENCE	ZID	—	80	100	125	Ω
HI-SPEED INPUT/OUTPUT CHARACTERISTICS (C-PHY)						
COMMON-POINT VOLTAGE HS RECEIVE MODE	VCPRX(DC)	—	95	—	390	mV
DIFFERENTIAL INPUT IMPEDANCE	Z _{ID_AB} Z _{ID_BC} Z _{ID_CA}	—	80	100	120	Ω
COMMON-POINT INTERFERENCE BEYOND 450 MHz	ΔV _{CPRX(HF)}	—	—	—	50	mV
COMMON-POINT INTERFERENCE 50MHz ~ 450MHz	ΔV _{CPRX(LF)}	—	-25	—	25	mV
DIFFERENTIAL INPUT HIGH THRESHOLD	V _{IDTH}	—	—	—	40	mV
DIFFERENTIAL INPUT LOW THRESHOLD	V _{IDTL}	—	-40	—	—	mV
SINGLE-ENDED INPUT HIGH VOLTAGE	V _{IHHS}	—	—	—	535	mV
SINGLE-ENDED INPUT LOW VOLTAGE	V _{ILHS}	—	-40	—	—	mV
SINGLE-ENDED THRESHOLD FOR HS TERMINATION ENABLE	V _{TERM-EN}	—	—	—	450	mV
COMMON-POINT TERMINATION	C _{CP}	—	—	—	90	pF



5.1.2 MIPI C-PHY DC CHARACTERISTICS

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POWER SUPPLY VOLTAGE FOR MIPI INTERFACE						
POWER SUPPLY VOLTAGE FOR MIPI INTERFACE	LVDSVDD	—	1.08	1.3	1.35	V
LOW POWER MODE INPUT CHARACTERISTICS						
PAD SIGNAL VOLTAGE RANGE	V_I	—	-50	—	1350	mV
GROUND SHIFT	$V_{GND,SH}$	—	-50	—	50	mV
LOGIC 0 INPUT THRESHOLD	V_{IL}	—	—	—	550	mV
LOGIC 1 INPUT THRESHOLD	V_{IH}	—	740	—	—	mV
INPUT HYSTERESIS	V_{HYST}	—	25	—	—	mV
LPDT OUTPUT CHARACTERISTICS						
OUTPUT HIGH LEVEL	V_{OH}	—	0.95	1.25	1.3	V
OUTPUT LOW LEVEL	V_{OL}	—	-50	—	50	mV
LOGIC 0 CONTENTION THRESHOLD	$V_{IL,CD}$	—	0	—	200	mV
LOGIC 1 CONTENTION THRESHOLD	$V_{IH,CD}$	—	450	—	LVDSVDD	mV
HIGH-SPEED INPUT/OUTPUT CHARACTERISTICS						
SINGLE-END INPUT LOW VOLTAGE	$V_{IL,HS}$	—	-40	—	—	mV
SINGLE-END INPUT HIGH VOLTAGE	$V_{IH,HS}$	—	—	—	535	mV
SINGLE-END THRESHOLD FOR HS TERMINATION ENABLE	$V_{TERM-EN}$	—	—	—	450	mV
COMMON MODE VOLTAGE	$V_{CM,RSDC}$	—	95	250	390	mV
DIFFERENTIAL INPUT LOW THRESHOLD	$V_{ID,TL}$	—	-70	—	—	mV
DIFFERENTIAL INPUT HIGH THRESHOLD	$V_{ID,TH}$	—	—	—	70	mV
HI-SPEED TRANSMIT VOLTAGE	V_{OD}	—	140	200	250	mV
DIFFERENTIAL INPUT IMPEDENCE	Z_{ID-AB} Z_{ID-BC} Z_{ID-CA}	—	80	100	120	ohm
DIFFERENTIAL INPUT IMPEDENCE MISMATCH	ΔZ_{ID}	NOTE (1)	—	—	10	%

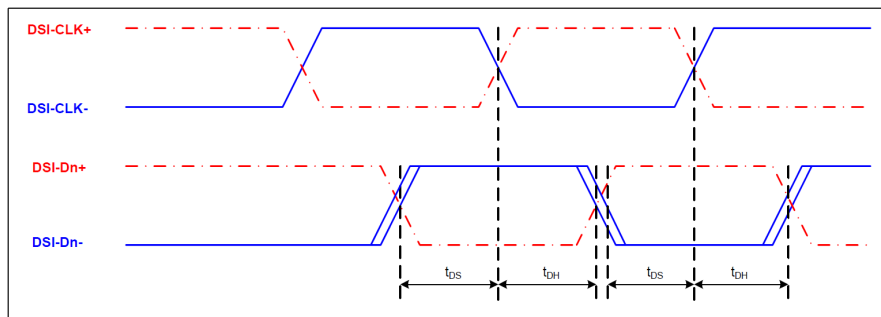
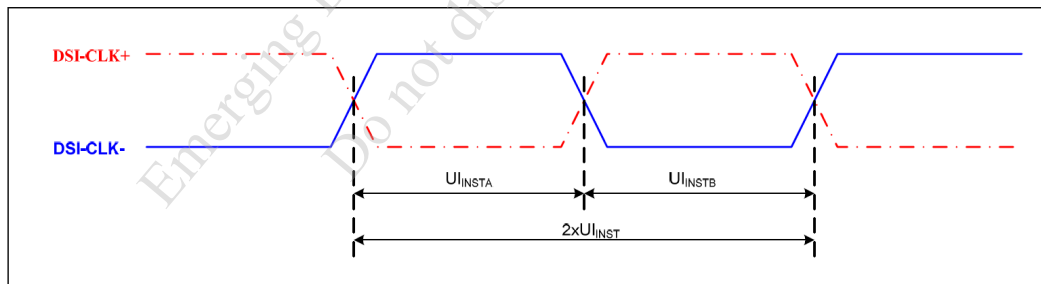
NOTE (1) : $\Delta Z_{ID}=3*[\max(Z_{ID-AB}, Z_{ID-BC}, Z_{ID-CA})-\min(Z_{ID-AB}, Z_{ID-BC}, Z_{ID-CA})]/(Z_{ID-AB} + Z_{ID-BC} + Z_{ID-CA})$

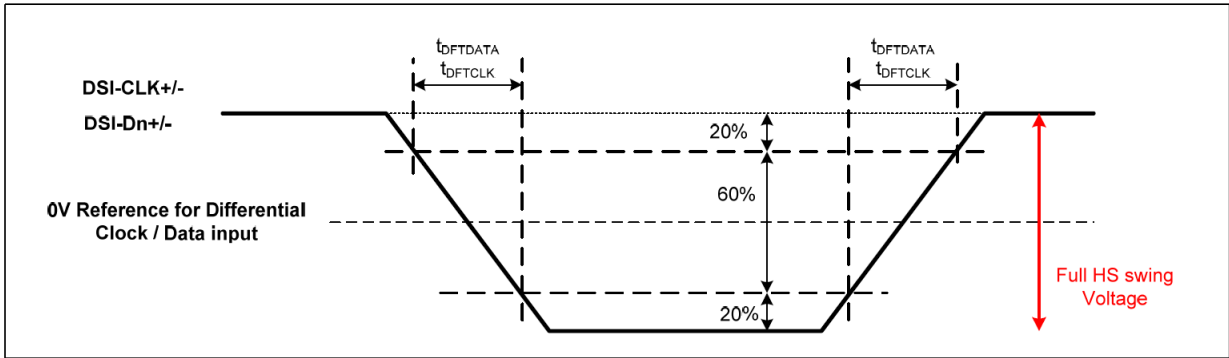


5.1.3 MIPI D-PHY AC CHARACTERISTICS

5.1.3.1 HIGH SPEED MODE

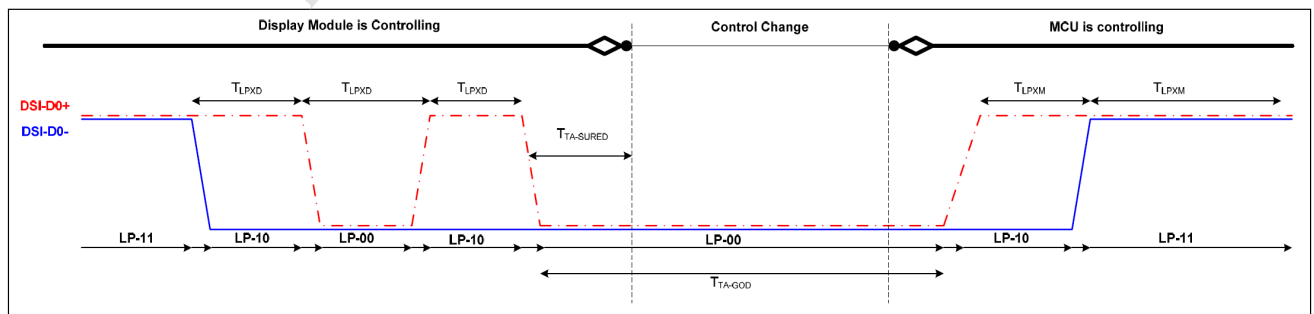
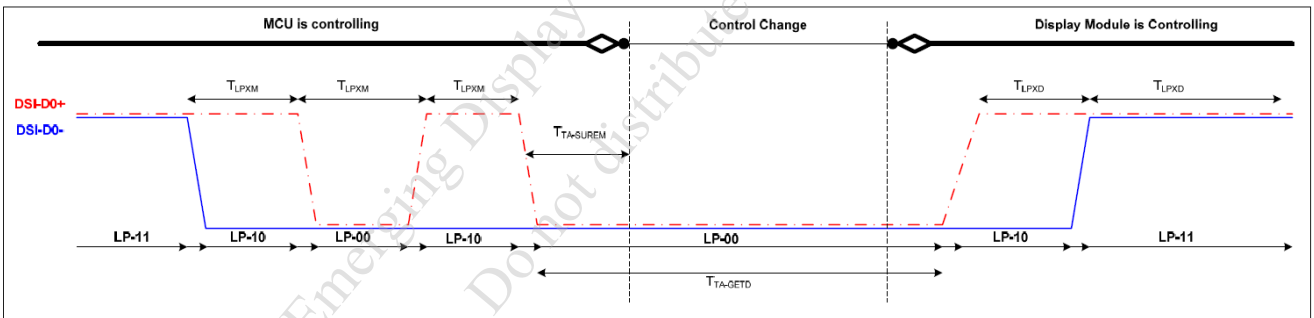
ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HIGH SPEED MODE						
DSI-CLK+/-	$2 \times UI_{INST}$	DOUBLE UI INSTANTANEOUS	1.54	—	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI INSTANTANEOUS HALFS	0.77	—	12.5	ns
DSI-Dn+/-	t_{DS}	DATA TO CLOCK SETUP TIME	0.15	—	—	UI
DSI-Dn+/-	t_{DH}	DATA TO CLOCK HOLD TIME	0.15	—	—	UI
DSI-CLK+/-	t_{DRTCLK}	DIFFERENTIAL RISE TIME FOR CLOCK	150	—	$0.3UI$	ps
DSI-Dn+/-	$t_{DRTDATA}$	DIFFERENTIAL RISE TIME FOR DATA	150	—	$0.3UI$	ps
DSI-CLK+/-	t_{DFTCLK}	DIFFERENTIAL FALL TIME FOR CLOCK	150	—	$0.3UI$	ps
DSI-Dn+/-	$t_{DFTDATA}$	DIFFERENTIAL FALL TIME FOR DATA	150	—	$0.3UI$	ps





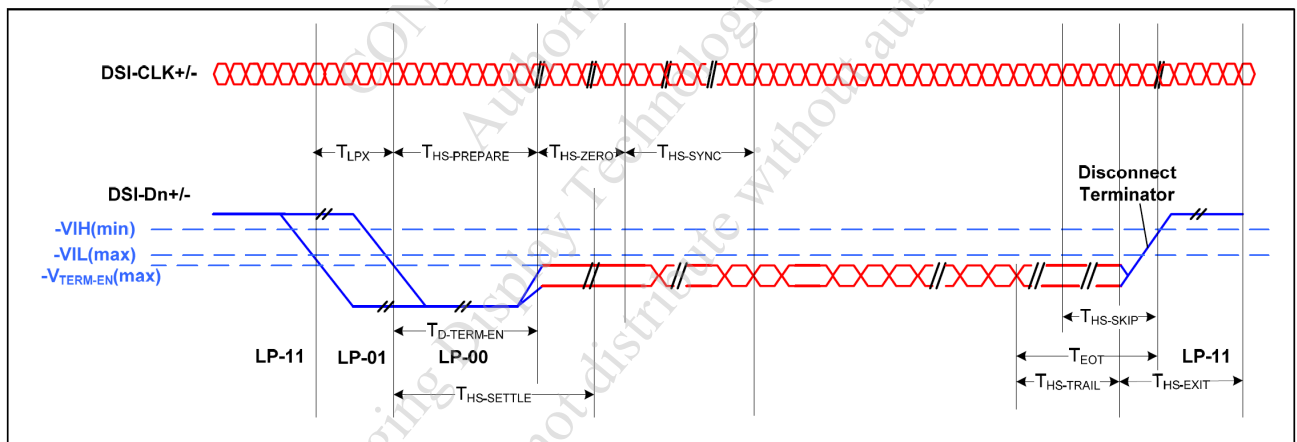
5.1.3.2 LOW POWER MODE

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOW POWER MODE						
DSI-D0+/-	T_{LPXM}	LENGTH OF LP-00, LP-01, LP-10 OR LP-11 PERIODS MPU DISPLAY MODULE	50	—	—	ns
DSI-D0+/-	T_{LPXD}	LENGTH OF LP-00, LP-01, LP-10 OR LP-11 PERIODS DISPLAY MODULE MPU	58	—	—	ns
DSI-D0+/-	$T_{TA-SURED}$	TIME-OUT BEFORE THE MPU START DRIVING	T_{LPXD}	—	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	TIME TO DRIVE LP-00 BY DISPLAY MODULE	$5XT_{LPXD}$	—	—	ns
DSI-D0+/-	T_{TA-GOD}	TIME TO DRIVE LP-00 AFTER TURNAROUND REQUEST - MPU	$4XT_{LPXD}$	—	—	ns
DSI-D0+/-	RATIO T_{LPX}	RATIO OF T_{LPXM} / T_{LPXD} BETWEEN MCU AND DISPLAY MODULE	2/3	—	3/2	—

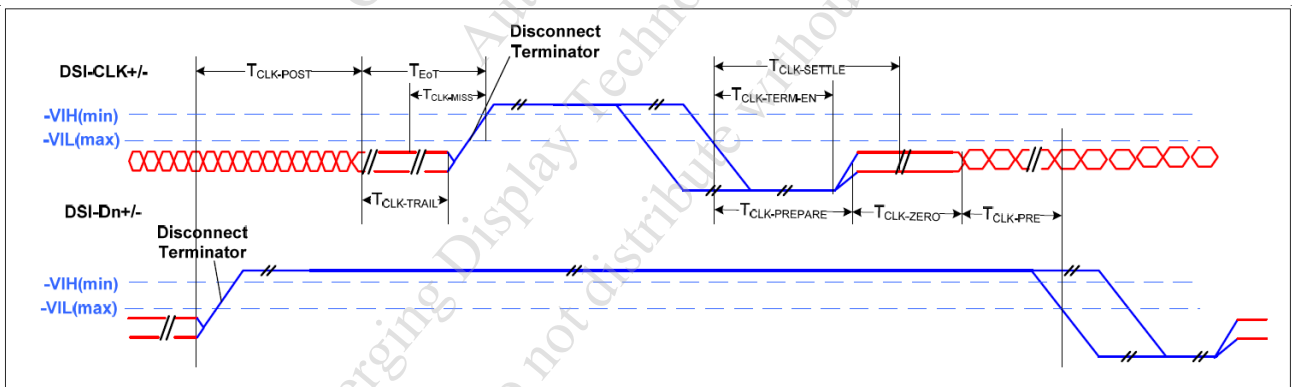


5.1.3.3 Bursts

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HIGH SPEED DATA TRANSMISSION BURSTS						
DSI-DN+/-	T_{LPX}	LENGTH OF ANY LOW-POWER STATE PERIOD	50	—	—	ns
DSI-DN+/-	$T_{HS-PREPARE}$	TIME TO DRIVE LP-00 TO PREPARE FOR HS TRANSMISSION	$40ns + 4UI$	—	$85ns + 6UI$	ns
DSI-DN+/-	$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + TIME TO DRIVE HS-0 BEFORE THE SYNC SEQUENCE	$145ns + 10UI$	—	—	ns
DSI-DN+/-	$T_{D-TERM-EN}$	TIME TO ENABLE DATA LANE RECEIVER LINE TERMINATION MEASURED FROM WHEN DN CROSSES $V_{IL(MAX)}$	TIME FOR DN TO REACH $V_{T_{ERM-EN}}$	—	$35ns + 4UI$	ns
DSI-DN+/-	$T_{HS-SKIP}$	TIME-OUT AT RX TO IGNORE TRANSITION PERIOD OF EOT	40	—	$55ns + 4UI$	ns
DSI-DN+/-	$T_{HS-TRAIL}$	TIME TO DRIVE FLIPPED DIFFERENTIAL STATE AFTER LAST PAYLOAD DATA BIT OF A HS TRANSMISSION BURST	MAX (8UI, $60ns + 4UI$)	—	—	ns
DSI-DN+/-	$T_{HS-EXIT}$	TIME TO DRIVE LP-11 AFTER HS BURST	100	—	—	ns
DSI-DN+/-	T_{EOT}	TIME FROM START OF $T_{HS-TRAIL}$ PERIOD TO START OF LP-11 STATE	—	—	$105ns + 12UI$	ns



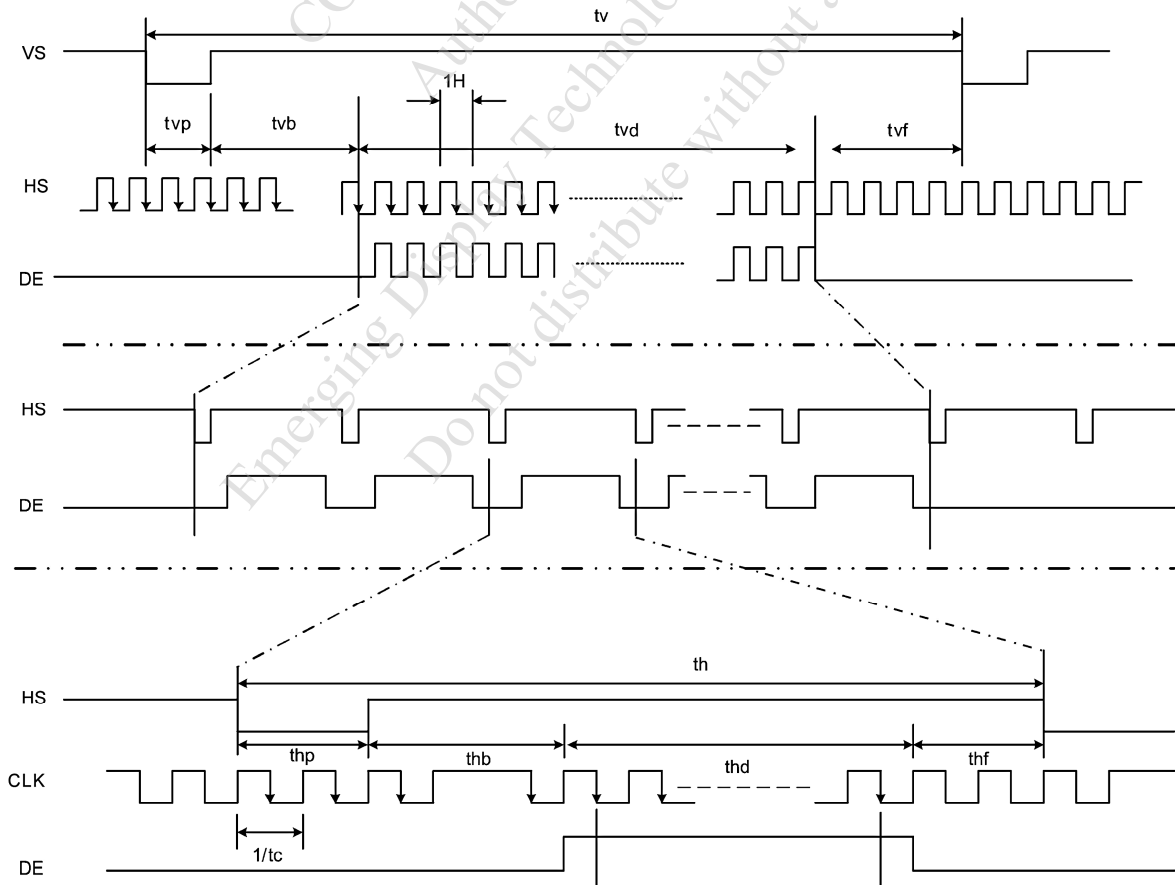
ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SWITCHING THE CLOCK LANE BETWEEN CLOCK TRANSMISSION AND LOW POWER MODE						
DSI-CLK+/-	$T_{CLK-POST}$	TIME THAT THE TRANSMITTER SHALL CONTINUE SENDING HS CLOCK AFTER THE LAST ASSOCIATED DATA LANE HAS TRANSITIONED TO LP MODE	$60ns + 52UI$	—	—	ns
DSI-CLK+/-	$T_{CLK-PRE}$	TIME THAT THE HS CLOCK SHALL BE DRIVEN PRIOR TO ANY ASSOCIATED DATA LANE BEGINNING THE TRANSITION FROM LP TO HS MODE	8	—	—	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	TIME TO DRIVE LP-00 TO PREPARE FOR HS CLOCK TRANSMISSION	38	—	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	TIME TO ENABLE CLOCK LANE RECEIVER LINE TERMINATION MEASURED FROM WHEN DN CROSSES $V_{IL(MAX)}$	TIME FOR DN TO REACH $V_{TERM-EN}$	—	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + TIME FOR LEAD HS-0 DRIVE PERIOD BEFORE STARTING CLOCK	300	—	—	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	TIME TO DRIVE HS DIFFERENTIAL STATE AFTER LAST PAYLOAD CLOCK BIT OF A HS TRANSMISSION BURST	60	—	—	ns
DSI-CLK+/-	T_{EoT}	TIME FROM START OF $T_{CLK-TRAIL}$ PERIOD TO START OF LP-11 STATE	—	—	$105ns + 12UI$	ns



5.1.4 TIMING FOR DSI VIDEO MODE

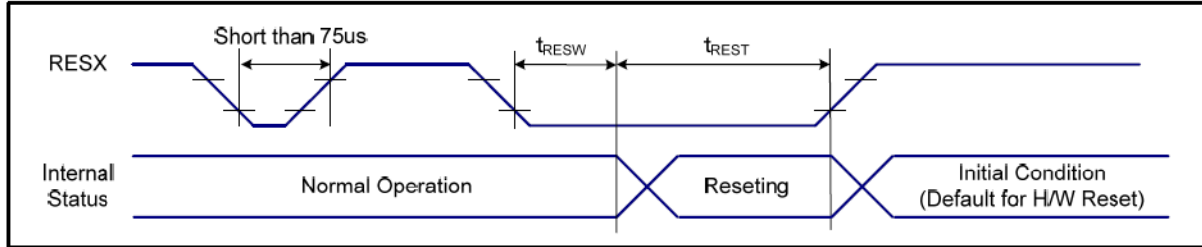
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLOCK CYCLE	$f_{CLK}^{(1)}$	—	151	—	MHz
HSYNC CYCLE	$1/t_h$	—	120.99	—	KHz
VSYNC CYCLE	$1/t_v$	—	59.98	—	Hz
HORIZONTAL SIGNAL					
HORIZONTAL CYCLE	t_h	—	1248	—	CLK
HORIZONTAL DISPLAY PERIOD	t_{hd}	—	1200	—	CLK
HORIZONTAL FRONT PORCH	t_{hf}	—	20	—	CLK
HORIZONTAL PULSE WIDTH	t_{hp}	—	10	—	CLK
HORIZONTAL BACK PORCH	t_{hb}	—	18	—	CLK
VERTICAL SIGNAL					
VERTICAL CYCLE	t_v	—	2017	—	H ⁽¹⁾
VERTICAL DISPLAY PERIOD	t_{vd}	—	1920	—	H ⁽¹⁾
VERTICAL FRONT PORCH	t_{vf}	—	53	—	H ⁽¹⁾
VERTICAL PULSE WIDTH	t_{vp}	—	12	—	H ⁽¹⁾
VERTICAL BACK PORCH	t_{vb}	—	32	—	H ⁽¹⁾

NOTE : 1.Unit: CLK=1/ f_{CLK} , H= t_h ,



5.2 RESET TIMING CHARACTERISTICS

t_{RESW} SHORTER THAN 75 μ s, RESET WILL BE REJECTED.



ITEM	SYMBOL	MIN.	TYP.	MAX.	NOTE	UNIT
*1) RESET LOW PULSE MINIMUM WIDTH	t_{RESW}	150	—	—	RESET SIGNAL RECOGNIZED	μ s
*2) RESET COMPLETE TIME	t_{REST}	5	—	120	RESET ACTION COMPLETE	ms

NOTE(1) : RESX LOW PULSE THAT IS TOO SHORT DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE TABLE BELOW.

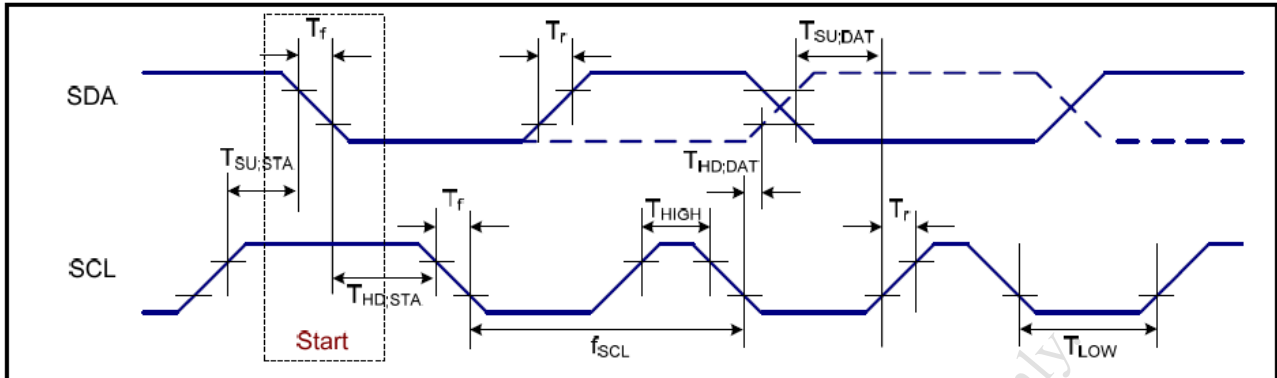
RESX PULSE	ACTION
SHORTER THAN 75 μ s	RESET REJECTED
LONGER THAN 150 μ s	RESET RECOGNIZED
BETWEEN 75 μ s AND 150 μ s	RESET SEQUENCE STARTS (IT DEPENDS ON VOLTAGE AND TEMPERATURE CONDITION.)

NOTE(2) : ONCE RESET LOW PULSE IS RECOGNIZED, SYSTEM REQUIRES RESX REMAINING LOW FOR ANOTHER 5ms TO COMPLETE H/W RESET.

NOTE(3) : DURING H/W RESET FLOW, ID0 ~ ID4 AND VCOM VALUE IN OTP WILL BE LATCHED TO INTERNAL REGISTER DURING THIS PERIOD. THIS LOADING IS DONE EVERY TIME WHEN H/W RESET IS COMPLETE ; THE H/W RESET SEQUENCE IS COMPLETE WHEN RESX IS REMAINING LOW LONGER THAN $t_{RESW} + t_{REST}$.

NOTE(4) : IT IS NECESSARY TO WAIT 15msec AFTER RELEASING RESX BEFORE SENDING COMMANDS. ALSO SLEEP OUT COMMAND CANNOT BE SENT FOR 120 msec.

5.3 I²C INTERFACE CHARACTERISTICS



ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL CLOCK FREQUENCY	f_{SCLK}	—	10	—	400	kHz
SCL CLOCK LOW PERIOD	T_{LOW}	—	1.2	—	—	us
SCL CLOCK HIGH PERIOD	T_{HIGH}	—	0.6	—	—	us
DATA SET-UP TIME	$T_{SU,DATA}$	—	250	—	—	ns
DATA HOLD TIME	$T_{HD,DATA}$	—	0	—	0.9	us
SCL AND SDA RISE TIME	T_r	NOTE (2)	$20+0.1C_b$	—	300	ns
SCL AND SDA FALL TIME	T_f	NOTE (2)	$20+0.1C_b$	—	300	ns
SDA FALL TIME FOR READ OUT	T_f	—	$20+0.1C_b$	—	1000	ns
CAPACITIVE LOAD REPRESENTED BY EACH BUS LINE	C_b	—	—	—	400	pF
SETUP TIME FOR A REPEATED START CONDITION	$T_{SU,STA}$	—	0.6	—	—	us
START CONDITION HOLD TIME	$T_{HD,STA}$	—	0.6	—	—	us
SETUP TIME FOR STOP CONDITION	$T_{SU,STO}$	—	0.6	—	—	us
TOLERABLE SPIKE WIDTH ON BUS	T_{SW}	NOTE (1)	—	—	50	ns
BUS FREE TIME BETWEEN A STOP AND START CONDITION	T_{BUF}	—	4.7	—	—	us

NOTE(1) : THE DEVICE INPUTS SDA AND SCL ARE FILTERED AND WILL REJECT SPIKES ON THE BUS LINES OF WIDTH $<T_{SW}(MAX)$.

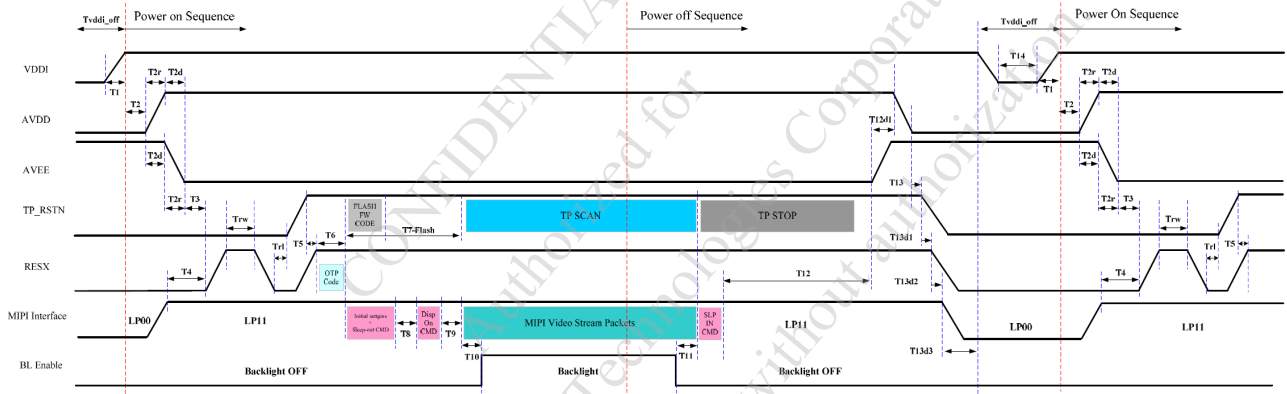
NOTE(2) : THE RISE AND FALL TIMES SPECIFIED HERE REFER TO THE DRIVER DEVICE AND ARE PART OF THE GENERAL FAST I²C-BUS SPECIFICATION. C_b = CAPACITIVE LOAD PER BUS LINE.

NOTE(3) : ALL TIMING VALUES ARE VALID WITHIN THE OPERATING SUPPLY VOLTAGE AND AMBIENT TEMPERATURE RANGES AND ARE REFERENCED TO V_{IL} AND V_{IH} WITH AN INPUT VOLTAGE SWING OF V_{SS} TO V_{DD1}

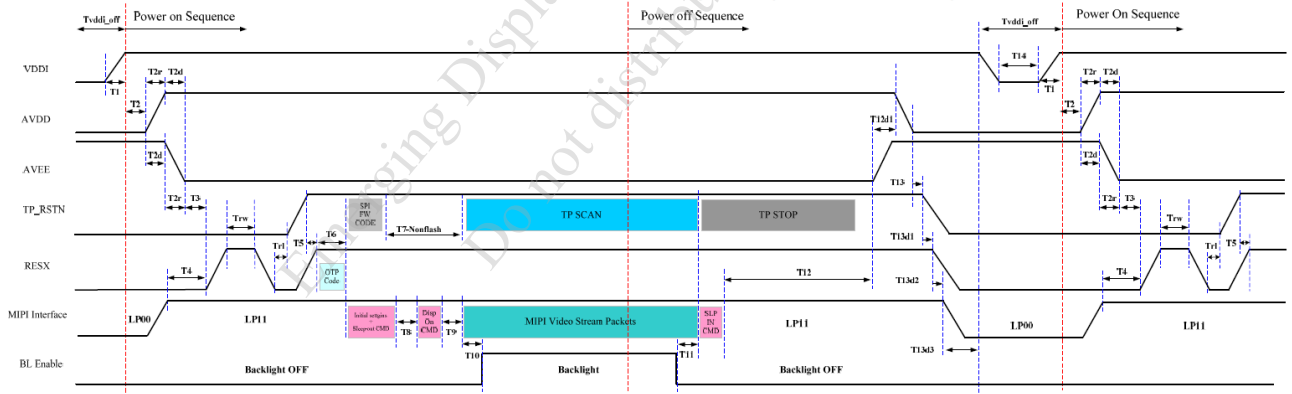
5.4 POWER ON/OFF SEQUENCE

- (1) THERE WILL BE NO HARD-DAMAGE TO THE DISPLAY MODULE IF THE POWER SEQUENCES ARE NOT MET.
- (2) THERE WILL BE NO ABNORMAL VISIBLE EFFECTS ON THE DISPLAY PANEL DURING THE POWER ON/OFF SEQUENCES.
- (3) THERE WILL BE NO ABNORMAL VISIBLE EFFECTS ON THE DISPLAY BETWEEN END OF POWER ON SEQUENCE AND BEFORE RECEIVING SLEEP-OUT COMMAND. ALSO BETWEEN RECEIVING SLEEP-IN COMMAND AND POWER OFF SEQUENCE.
- (4) RESX AND TP_RSTN MUST BE HELD STABLY BY HOST DURING POWER ON SEQUENCE, OTHERWISE FUNCTION IS NOT GUARANTEED.
- (5) DURING ABNORMAL POWER DROPPING, VDDI CAN START POWER DOWN 3ms AFTER AVDD/AVEE POWER DOWN.
- (6) ENABLE TIMING IS FOR REFERENCE ONLY AND NOT RESTRICTED (T10/T11).
- (7) 2nd RESET TIMING IS REQUESTED FOR RESX ASSERTION AND IS OPTIONAL FOR TP_RSTN ASSERTION.
- (8) ALL INPUT SIGNALS SHOULD BE KEPT GND, FLOATING OR LP00 STATUS DURING T_{VDDI_OFF}.

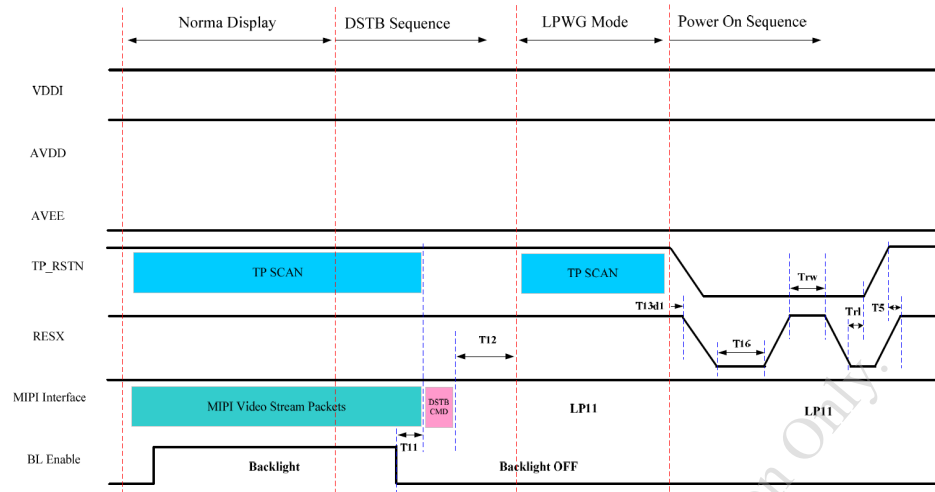
3 Power mode: Power On/Off Sequence (Flash Mode)



3 Power mode: Power On/Off Sequence (Non-Flash Mode)



TP Gesture Mode Exit Sequence



ITEM	DESCRIPTIONS	MIN.	TYP.	MAX.	UNIT
T1	RISE TIME FROM 0.1*VDD TO 0.9*VDD	0	—	5	ms
T2	AVDD POWER UP AFTER VDD POWER ON	3	—	—	ms
T2d	AVEE POWER UP AFTER AVDD POWER UP	0	—	—	ms
T2r	RISE TIME FROM 0.1*AVDD TO 0.9*AVDD RISE TIME FROM 0.1*AVEE TO 0.9*AVEE	0.1	—	5	ms
T3	RESX RESET RELEASE TIME AFTER AVDD/AVEE POWER ON	5	—	—	ms
T4	MIPI SIGNALS START (HI-Z/GND TO LP11) TO RESX RISING EDGE	0	—	—	ms
T5	TP RESET RELEASE TO LCD RESET RELEASE	0	—	—	ms
T6	FLASH/OTP SETTINGS DOWNLOAD FINISHED AFTER RESX RELEASED MIPI IF MAY START TO SEND INITIAL SETTINGS + SLEEP-OUT CMD SPI IF MAY START TO SEND FW CODE	—	—	35	ms
T7-Nonflash	SPI FW CODE DOWNLOAD FINISH TO TP SCAN START (NON-FLASH MODE)	—	—	200	ms
T7-Flash	FLASH FW CODE DOWNLOAD START TO TP SCAN START (FLASH MODE)	—	—	280	ms
T8	SLEEP-OUT CMD TO DISPLAY-ON CMD	—	120	—	ms
T9	DISPLAY-ON CMD TO MIPI VIDEO STREAM ON TIM	10	—	—	ms
T10	MIPI VIDEO STREAM ON TIME TO BACKLIGHT ON TIME	100	—	—	ms
T11	BACKLIGHT OFF TIME TO MIPI VIDEO STREAM OFF TIME	100	—	—	ms
T12	AVEE POWER DOWN AFTER SLEEP-IN CMD	150	—	—	ms
T12d1	AVDD POWER DOWN AFTER AVEE POWER DOWN	0	—	—	ms
T13	TP_RSTN FALLING EDGE AFTER AVDD POWER DOWN	0	—	—	ms
T13d1	IN POWER OFF SEQUENCE, TP_RSTN FALLING EDGE TO RESX FALLING EDGE	0	—	—	ms
T13d2	IN POWER OFF SEQUENCE, RESX FALLING EDGE TO MIPI INTERFACE POWER DOWN	0	—	—	ms
T13d3	IN POWER OFF SEQUENCE, MIPI INTERFACE POWER DOWN TO VDDI POWER DOWN	3	—	—	ms
T14	VDDI RISE AGAIN AFTER VDDI POWER DOWN (0.1*VDD)	50	—	—	ms
T15	VGL POWER UP AFTER VGH POWER UP	0	—	—	ms
T15d	VGH / VGL POWER DOWN BEFORE AVDD/AVEE	0	—	—	ms
T16	RESX FALLING EDGE (EXIT FROM DSTB MODE) TO RESX RISING EDGE	5	—	120	ms
Trl	2ND RESX RESET LOW WIDTH TO TP_RSTN RISING	5	—	—	ms
Trw	RESX HIGH LEVEL WIDTH BEFORE 2ND RESX RESET	5	—	10	ms

6. OPTICAL CHARACTERISTICS (NOTE 1)

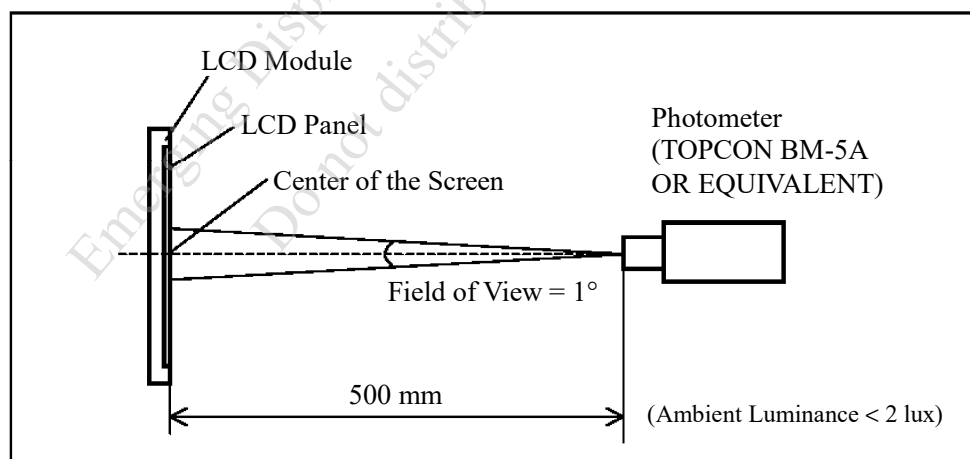
6.1 OPTICAL CHARACTERISTICS

Ta=25±2°C

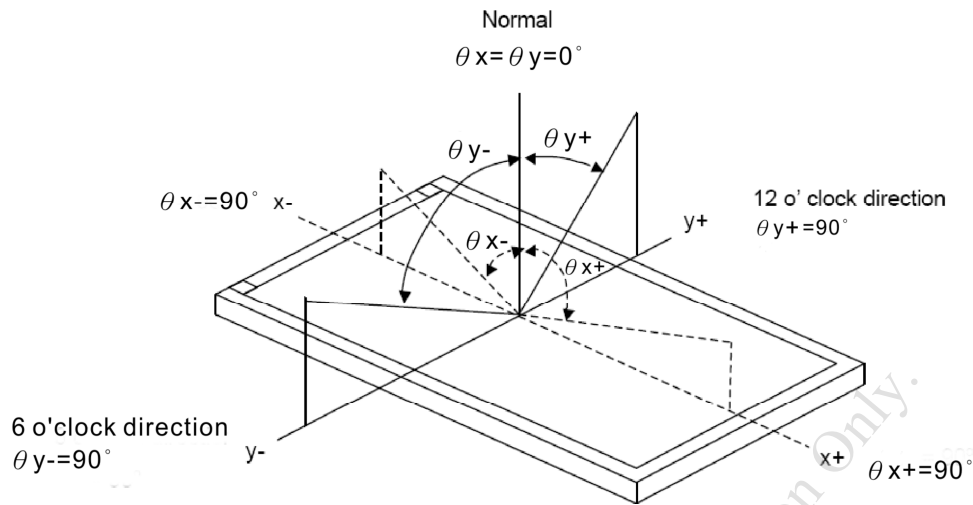
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK	
VIEWING ANGLE	θ_{y+}	CR ≥ 10	$\theta_x=0^\circ$	75	80	—	deg.	NOTE (2) NOTE (3)
	θ_{y-}			75	80	—		
	θ_{x+}		$\theta_y=0^\circ$	75	80	—		
	θ_{x-}			75	80	—		
CONTRAST RATIO(CENTER)	CR	$\theta_x=0^\circ, \theta_y=0^\circ$	1200	—	—	—	NOTE (3)	
RESPONSE TIME	Tr + Tf	$\theta_x=0^\circ, \theta_y=0^\circ$	—	25	50	msec	NOTE (4)	
COLOR CHROMATICITY (CENTER)	WHITE	Wx	$\theta_x=0^\circ, \theta_y=0^\circ$ NTSC : 72.3% VLED-VLSS =12.0V LED B/L=ON PWM=100%	0.27	0.32	0.37	—	NOTE (5)
		Wy		0.28	0.33	0.38		
	RED	Rx		0.63	0.68	0.73		
		Ry		0.31	0.36	0.41		
	GREEN	Gx		0.27	0.32	0.37		
		Gy		0.61	0.66	0.71		
	BLUE	Bx		0.12	0.17	0.22		
		By		0.03	0.08	0.13		
THE BRIGHTNESS OF MODULE (CENTER)	B		900	1000	—	cd/m ²	NOTE (6)	
THE UNIFORMITY OF MODULE	—		70	75	—	%	NOTE (7)	

NOTE (1) : TEST CONDITION :

AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES. MEASUREMENT SHOULD BE EXECUTED IN A STABLE, WINDLESS, AND DARK ROOM.



NOTE (2) : DEFINITION OF VIEWING ANGLE :



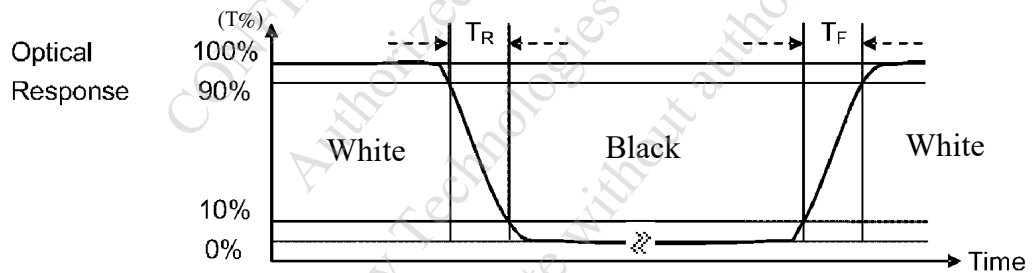
NOTE (3) : DEFINITION OF CONTRAST RATIO (CR) :

MEASURED AT THE CENTER POINT OF MODULE

$$\text{CONTRAST RATIO(CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

NOTE (4) : DEFINITION OF RESPONSE TIME : T_R AND T_F

THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



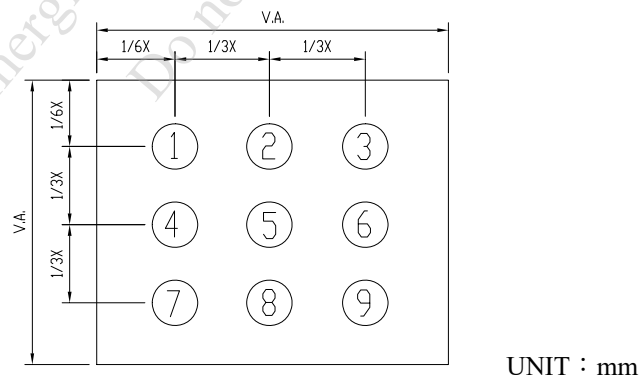
NOTE (5) : DEFINITION OF COLOR CHROMATICITY

(a) 100% RGB PIXEL DATA TRANSMISSION WHEN ALL THE INPUT TERMINALS OF MODULE ARE ELECTRICALLY POWERED ON.

(b) MEASURED AT THE CENTER POINT OF MODULE

NOTE (6) : MEASURED THE BRIGHTNESS OF WHITE STATE AT CENTER POINT.

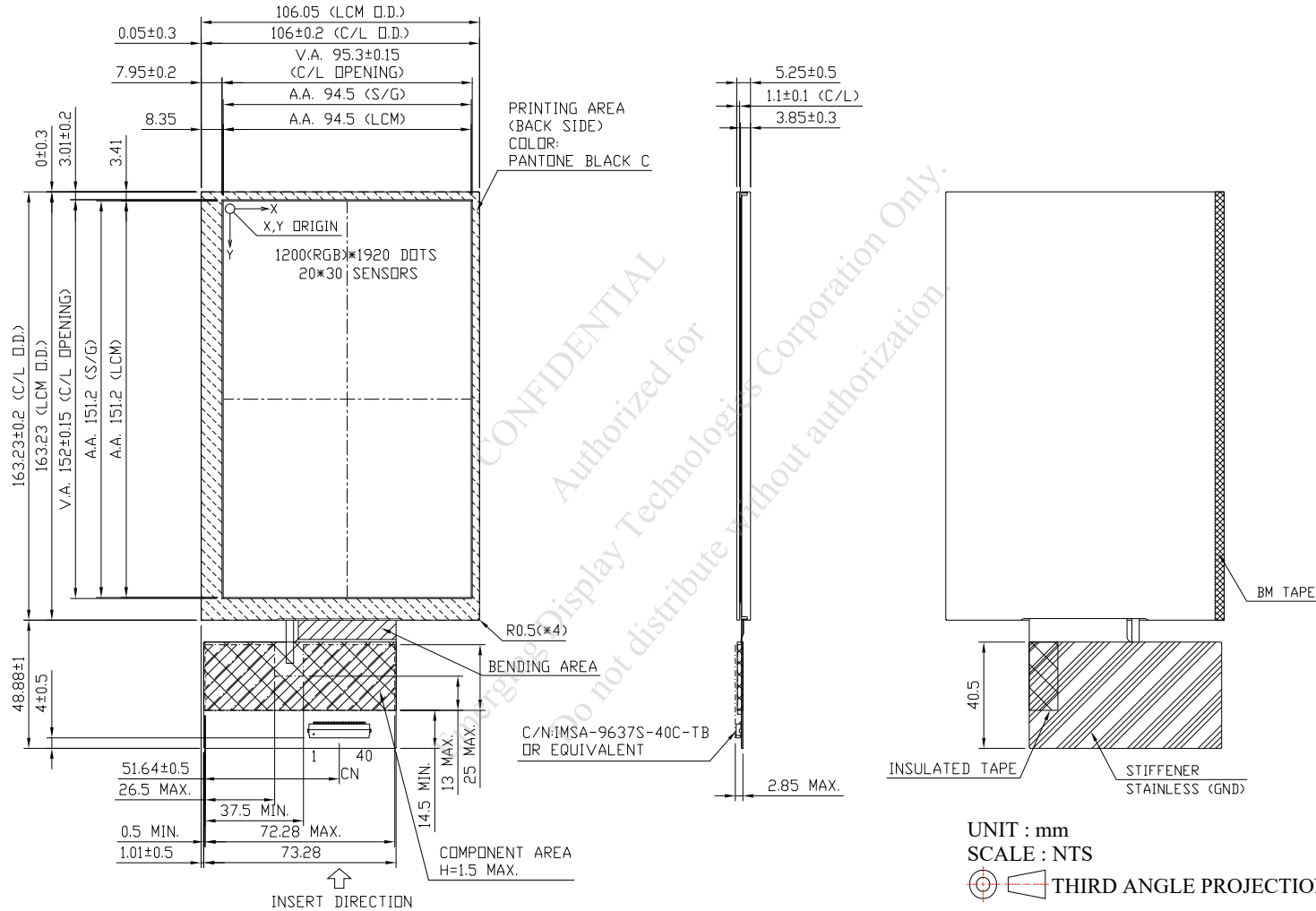
NOTE (7) : (a) DEFINITION OF BRIGHTNESS UNIFORMITY



(b) THE BRIGHTNESS UNIFORMITY CALCULATING METHOD

$$\text{UNIFORMITY} : \frac{\text{MINIMUM BRIGHTNESS}}{\text{MAXIMUM BRIGHTNESS}} * 100\%$$

7. OUTLINE DIMENSIONS



UNIT : mm
SCALE : NTS
THIRD ANGLE PROJECTION

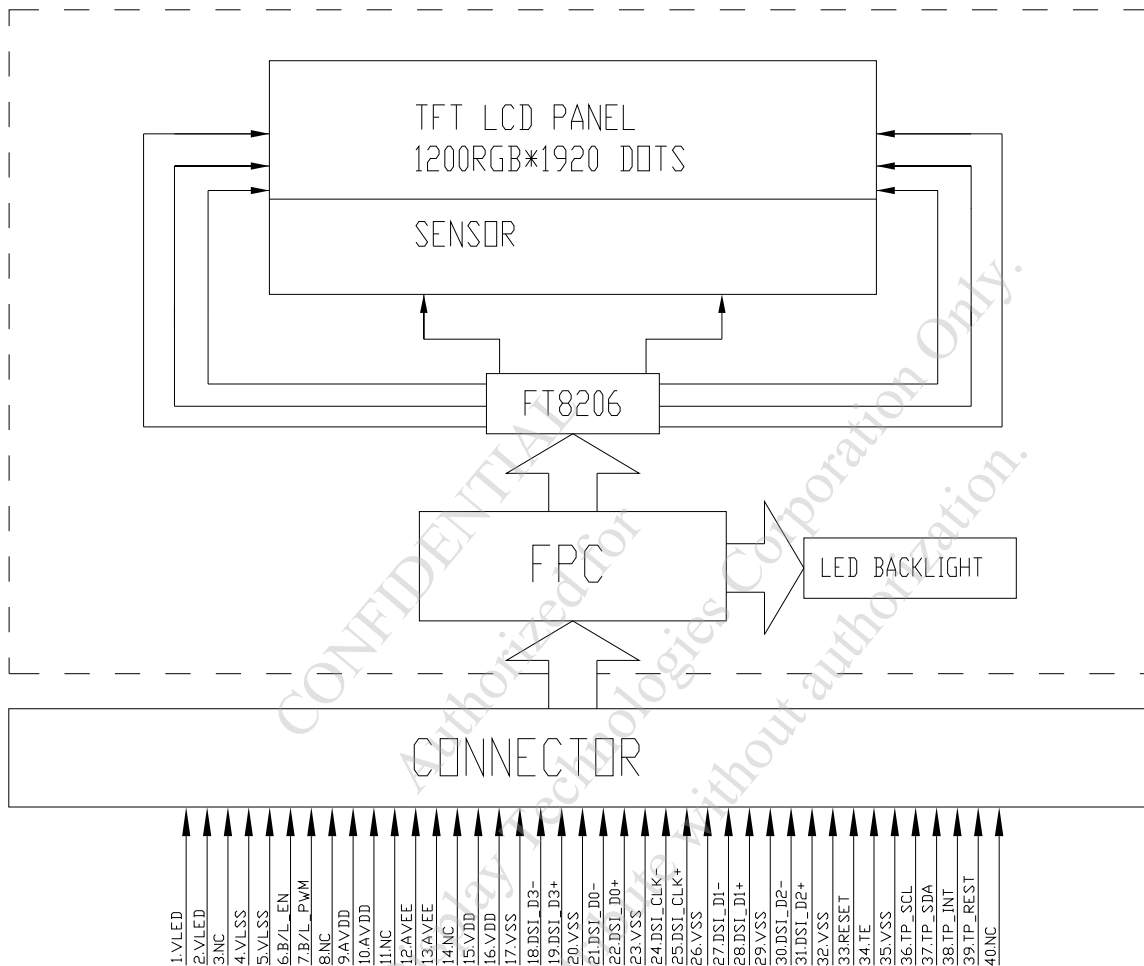
NOT SPECIFIED TOLERANCE IS ± 0.5

NOTE :

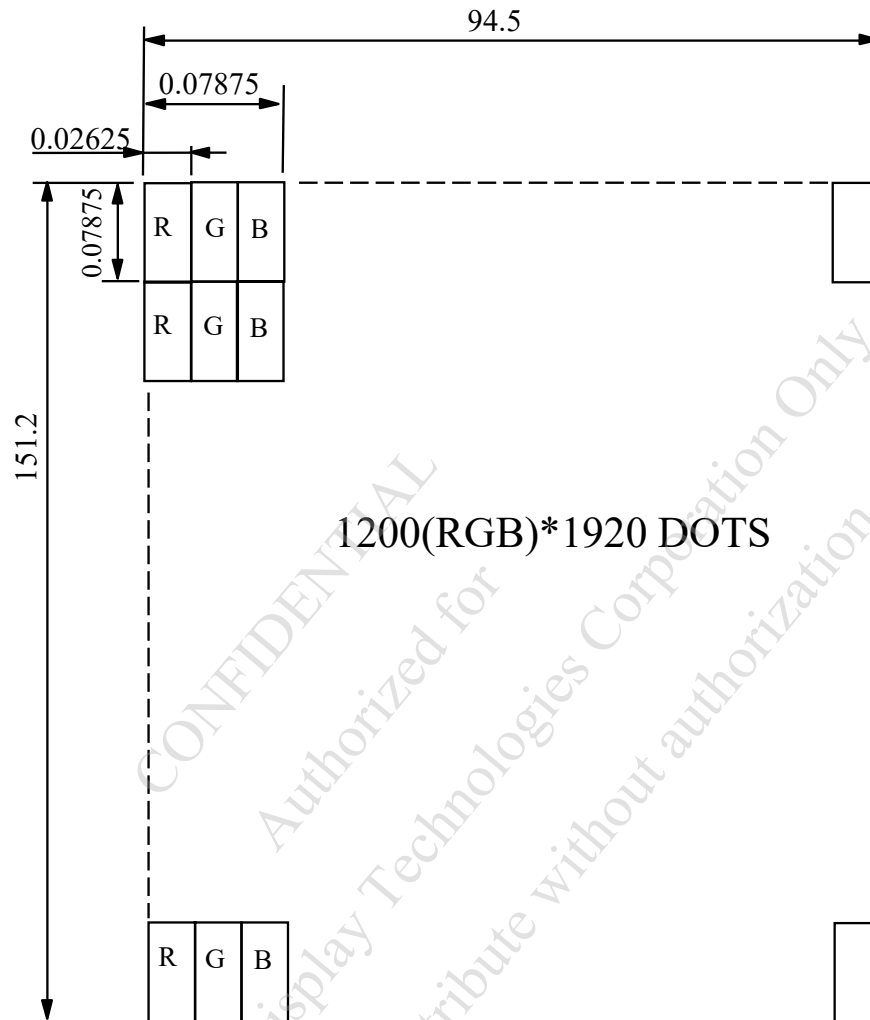
1. C/L GLASS : SODA LIME , CHAMFERED EDGES.
2. FPC BENDING RADIUS SHOULD BE MORE THAN 1.0 mm.

8. BLOCK DIAGRAM

8.1 TFT



9. DETAIL DRAWING OF DOT MATRIX



1200(RGB)*1920 DOTS

UNIT : mm

SCALE : NTS

NOT SPECIFIED TOLERANCE IS ± 0.1

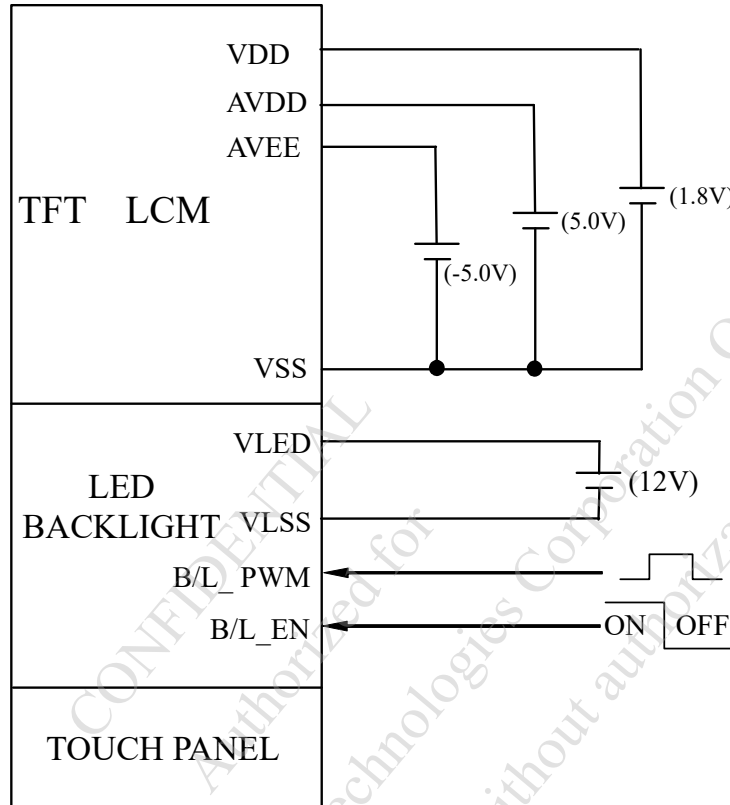
DOTS MATRIX TOLERANCE IS ± 0.01

10. INTERFACE SIGNALS

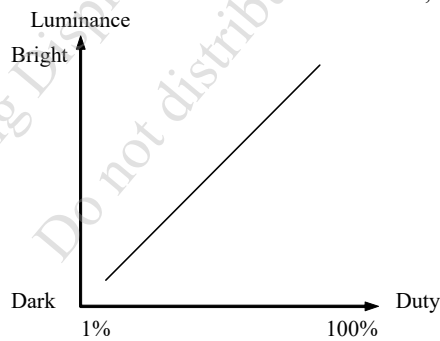
PIN NO.	SYMBOL	FUNCTION
1	VLED	LED BACKLIGHT ANODE
2	VLED	LED BACKLIGHT ANODE
3	NC	NON CONNECTION
4	VLSS	LED BACKLIGHT CATHODE
5	VLSS	LED BACKLIGHT CATHODE
6	B/L EN	LED ENABLE PIN
7	B/L PWM	ADJUST FOR LED BRIGHTNESS
8	NC	NON CONNECTION
9	AVDD	POWER SUPPLY VOLTAGE FOR ANALOG
10	AVDD	POWER SUPPLY VOLTAGE FOR ANALOG
11	NC	NON CONNECTION
12	AVEE	POWER SUPPLY VOLTAGE FOR ANALOG
13	AVEE	POWER SUPPLY VOLTAGE FOR ANALOG
14	NC	NON CONNECTION
15	VDD	LOGIC INPUT POWER
16	VDD	LOGIC INPUT POWER
17	VSS	GROUND
18	DSI D3-	MIPI DATA LANE3 INPUT(NEGATIVE)
19	DSI D3+	MIPI DATA LANE3 INPUT(POSITIVE)
20	VSS	GROUND
21	DSI D0-	MIPI DATA LANE0 INPUT(NEGATIVE)
22	DSI D0+	MIPI DATA LANE0 INPUT(POSITIVE)
23	VSS	GROUND
24	DSI CLK-	MIPI CLK INPUT(NEGATIVE)
25	DSI CLK+	MIPI CLK INPUT(POSITIVE)
26	VSS	GROUND
27	DSI D1-	MIPI DATA LANE1 INPUT(NEGATIVE)
28	DSI D1+	MIPI DATA LANE1 INPUT(POSITIVE)
29	VSS	GROUND
30	DSI D2-	MIPI DATA LANE2 INPUT(NEGATIVE)
31	DSI D2+	MIPI DATA LANE2 INPUT(POSITIVE)
32	VSS	GROUND
33	RESET	RESET LOW IS ACTIVE, NORMALLY PULLED HIGH
34	TE	TEARING EFFECT OUTPUT PIN
35	VSS	GROUND
36	TP_SCL	I2C CLOCK INPUT
37	TP_SDA	I2C DATA INPUT AND OUTPUT
38	TP_INT	EXTERNAL INTERRUPT TO THE HOST
39	TP_REST	EXTERNAL RESRT, LOW ACTIVE
40	NC	NON CONNECTION

11. POWER SUPPLY

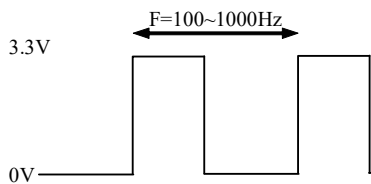
11.1 POWER SUPPLY FOR LCM



NOTE (1) : ADJUST THE PWM SIGNAL IN ORDER TO CONTROL LED BACKLIGHT'S BRIGHTNESS. THE HIGHER THE DUTY CYCLE, THE HIGHER THE BRIGHTNESS



NOTE (2) : PWM SIGNAL OPERATION FREQUENCY IS 100~1000Hz AND DIMMING DUTY.



PWM Dimming Frequency [Hz]	Dimming Duty	
	Min [%]	Max [%]
100 <math>< F_{DIM} < 200</math>	0.1	100
200 <math>< F_{DIM} < 500</math>	0.4	100
500 <math>< F_{DIM} < 1K</math>	0.8	100

12. CAPACITIVE TOUCH PANEL SPECIFICATION

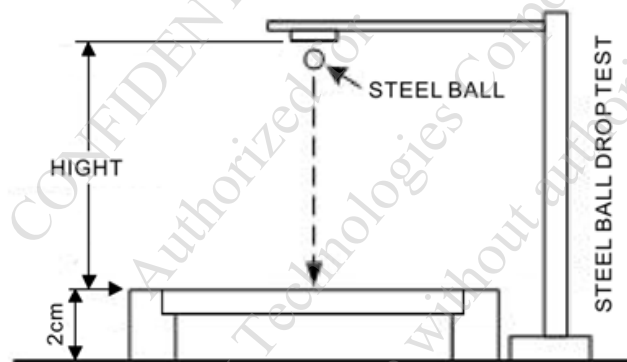
12.1 HARDNESS

ITEM	DESCRIPTION
SURFACE HARDNESS	(7)H (MIN.)

12.2 DURABILITY

USING STEEL BALL AND FALLING ON TOUCH PANEL SURFACE, FROM THE HEIGHT MUST PASS BELOW CONDITIONS :

ITEM	CONDITION	INSPECTION METHOD	DESCRIPTION
STEEL BALL DROP TEST	WEIGHT : 67g HEIGHT OF FALL : 30 cm	VISUAL INSPECTION	SIGN OF FRACTURE OR DAMAGE IS NOT ACCEPTABLE 3 TIME/ 1 POINTS, 25°C (CENTER POINT)

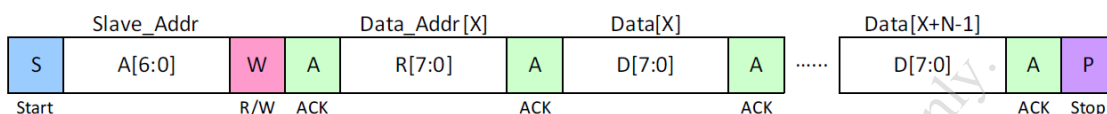


12.3 I2C INTERFACE DATA STRUCTURE

12.3.1 I2C READ/WRITE INTERFACE DESCRIPTION

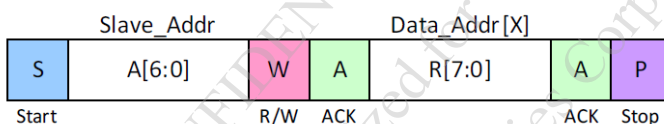
IT IS IMPORTANT TO NOTE THAT THE TP_I2C_SDA AND TP_I2C_SCL MUST CONNECT WITH A PULL-HIGH RESISTOR RESPECTIVELY BEFORE YOU READ/WRITE I2C DATA.

12.3.2 HOST WRITE DATA TO SLAVE

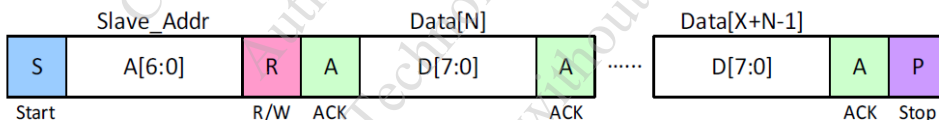


12.3.3 HOST READ DATA FROM SLAVE

Step1: Write Data Address

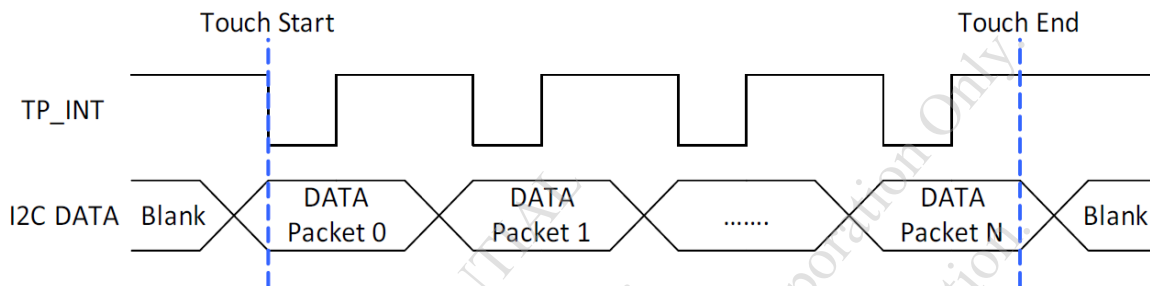


Step2: Read Data



12.3.4 INTERRUPT SIGNAL FORM CTPM TO HOST

AS FOR STANDARD CTPM, HOST NEEDS TO USE BOTH INTERRUPT SIGNAL AND I2C/SPI INTERFACE TO GET THE TOUCH DATA. CTPM WILL OUTPUT AN INTERRUPT REQUEST SIGNAL TO THE HOST WHEN THERE IS A VALID TOUCH. THEN HOST CAN GET THE TOUCH DATA VIA I2C/SPI INTERFACE. IF THERE IS NO VALID TOUCH DETECTED, THE TP_INT WILL OUTPUT HIGH LEVEL, AND THE HOST DOES NOT NEED TO READ THE TOUCH DATA. THE INTERRUPT TRIGGER MODE IS THE FALLING-EDGE TRIGGER MODE.



WHILE FOR INTERRUPT TRIGGER MODE, TP_INT SIGNAL WILL BE SET TO LOW IF THERE IS A TOUCH DETECTED. BUT WHENEVER AN UPDATE OF VALID TOUCH DATA, CTPM WILL PRODUCE A VALID PULSE ON TP_INT PORT FOR TP_INT SIGNAL, AND HOST CAN READ THE TOUCH DATA PERIODICALLY ACCORDING TO THE FREQUENCY OF THIS PULSE. IN THIS MODE, THE PULSE FREQUENCY IS THE TOUCH DATA UPDATING RATE.

WHILE DETECT THE FALLING EDGE OF TP_INT PORT, HOST CAN READ TOUCH DATA FROM REGISTER 0X01 OF WORK MODE, THEN PARSE AND COMBINE TOUCH DATA INTO X/Y COORDINATES AND OTHER ATTRIBUTES, PLEASE REFERS TO THE REGISTER MAP FOR DETAILS.

13 INSPECTION CRITERIA

13.1 APPLICATION

THIS INSPECTION STANDARD IS TO BE APPLIED TO THE LCD MODULE DELIVERED FROM EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) TO CUSTOMERS

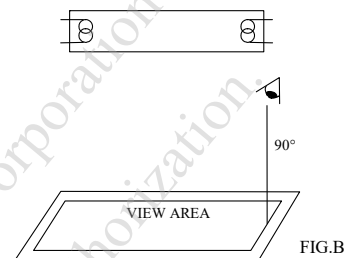
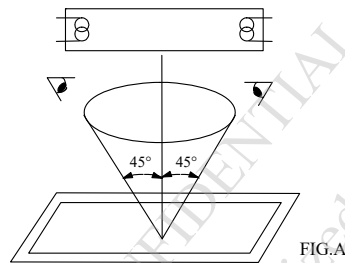
13.2 INSPECTION CONDITIONS

13.2.1 (1)OBSERVATION DISTANCE : 45 ± 5 cm

(2)VIEWING ANGLE : $\pm 45^\circ$

$\pm 45^\circ$ (FOR SECTION WITHIN VIEWING AREA), REFER TO FIG.A
90° (FOR SECTION OUTSIDE OF VIEWING AREA), REF TO FIG.B
PERPENDICULAR TO MODULE SURFACE

VIEWING ANGLE SHOULD BE SMALLER THAN 45°



THE INSPECTION CRITERIA IS ACCORDING TO LINE OF SIGHT. INSPECTION SHALL BE MADE WITHIN THE HALF SECTION OF THE VIEWING CONE GENERATED BY LINE SEGMENT OF 45° WITH RESPECT TO THE VERTICAL AXIS FROM CENTER VERTEX OF LCD, THE FLUORESCENT LAMP AND THE CONE AXIS MUST BE PERPENDICULAR TO THE LCD SURFACE.

IF THE DEFECTS ARE OUTSIDE OF VIEWING AREA, IT SHALL BE INSPECTED BY 90° WITH RESPECT TO THE VERTICAL AXIS FROM EDGE OF VIEWING AREA.

13.2.2 ENVIRONMENT CONDITIONS :

AMBIENT TEMPERATURE		$25 \pm 5^\circ\text{C}$
AMBIENT HUMIDITY		$65 \pm 20\% \text{RH}$
AMBIENT ILLUMINATION	COSMETIC INSPECTION	600~800 lux
	FUNCTIONAL INSPECTION	200~500 lux
INSPECTION TIME		15 secs

13.2.3 INSPECTION LOT

QUANTITY PER DELIVERY LOT FOR EACH MODEL

13.2.4 INSPECTION METHOD

A SAMPLING INSPECTION SHALL BE MADE ACCORDING TO THE FOLLOWING PROVISIONS TO JUDGE THE ACCEPTABILITY

(a)APPLICABLE STANDARD :



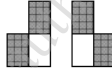
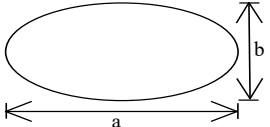
ANSI/ ASQ Z1.4 NORMAL INSPECTION LEVEL II

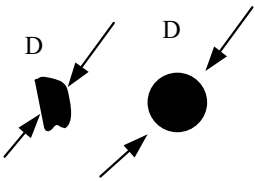
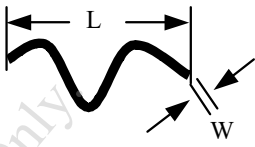
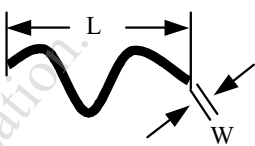
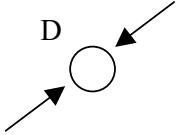
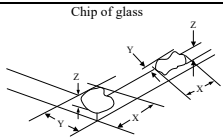
(b)AQL : MAJOR DEFECT : AQL 0.65

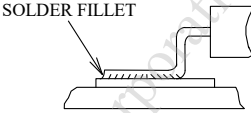
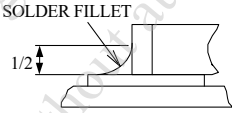
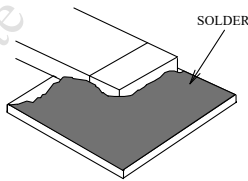
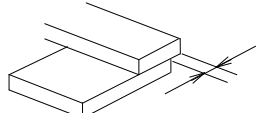
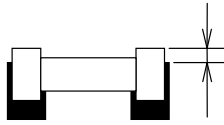
MINOR DEFECT : AQL 1.0

13.3 DEFECTS CLASSIFICATION

TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	<ul style="list-style-type: none"> • DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS EX: DISCONNECTION, SHORT CIRCUIT ETC 	0.65
	2.CTP FUNCTION	<ul style="list-style-type: none"> • NO FUNCTION • BROKEN LINE • FALSE TOUCH 	
	3.BACKLIGHT	<ul style="list-style-type: none"> • NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION 	
	4.DIMENSIONS	<ul style="list-style-type: none"> • SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS 	
MINOR DEFECT	1.DISPLAY ZONE	<ul style="list-style-type: none"> • BLACK/WHITE SPOT • BUBBLES ON POLARIZER • NEWTON RING • BLACK/WHITE LINE • SCRATCH • CONTAMINATION • UNEVEN COLOR SPREAD 	1.0
	2.BEZEL ZONE	<ul style="list-style-type: none"> • STAINS • SCRATCHES • FOREIGN MATTER 	
	3.SOLDERING	<ul style="list-style-type: none"> • INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS 	
	4.DISPLAY ON (ALL ON)	<ul style="list-style-type: none"> • LIGHT LINE 	

NO.	ITEM	CRITERIA																								
1	DISPLAY ON INSPECTION	1. INCORRECT PATTERN 2. MISSING SEGMENT 3. DIM SEGMENT 4. OPERATING VOLTAGE BEYOND SPEC																								
2	OVERALL DIMENSIONS	1. OVERALL DIMENSION BEYOND SPEC																								
3	DOT DEFECT	<p>(1) INSPECTION PATTERN: FULL WHITE, FULL BLACK, RED, GREEN AND BLUE SCREENS.</p> <p>(2)</p> <table border="1" data-bbox="584 622 1171 734"> <thead> <tr> <th>DEFECT TYPE</th> <th>CRITERIA</th> </tr> </thead> <tbody> <tr> <td>BRIGHT DOT</td> <td>$N \leq 3$</td> </tr> <tr> <td>DARK DOT</td> <td>$N \leq 3$</td> </tr> <tr> <td>TOTAL BRIGHT AND DARK DOT</td> <td>$N \leq 6$</td> </tr> </tbody> </table> <p>NOTE :</p> <p>1. DEFINITION OF DOT DEFECT INDUCED FROM THE PANEL INSIDE</p> <p>(A) BRIGHT DOT : DOTS APPEAR BRIGHT AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER BLACK PATTERN.</p> <p>(B) DARK DOT : DOTS APPEAR DARK AND UNCHANGED IN SIZE IN WHICH LCD PANEL IS DISPLAYING UNDER PURE RED, GREEN, BLUE PICTURE.</p> <p>(C) 2 DOT ADJACENT = 1 PAIR = 2 DOTS</p> <p>PICTURE:</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  <p>2 dot adjacent</p> </div> <div style="text-align: center;">  <p>2 dot adjacent (vertical)</p> </div> <div style="text-align: center;">  <p>2 dot adjacent (slant)</p> </div> </div>	DEFECT TYPE	CRITERIA	BRIGHT DOT	$N \leq 3$	DARK DOT	$N \leq 3$	TOTAL BRIGHT AND DARK DOT	$N \leq 6$																
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4	BUBBLES OF POLARIZER /DIRT/CF FAIL /SURFACE STAINS	<table border="1" data-bbox="576 1182 1331 1491"> <thead> <tr> <th></th> <th>AVERAGE DIAMETER (mm) : D</th> <th>NUMBER OF PIECES PERMITTED</th> </tr> </thead> <tbody> <tr> <td rowspan="3">BUBBLE ON THE POLARIZER</td> <td>$D \leq 0.15$</td> <td>IGNORE</td> </tr> <tr> <td>$0.15 < D \leq 0.5$</td> <td>$N \leq 4$</td> </tr> <tr> <td>$0.5 < D$</td> <td>NONE</td> </tr> <tr> <td rowspan="3">SURFACE STAINS</td> <td>$D \leq 0.15$</td> <td>IGNORE</td> </tr> <tr> <td>$0.15 < D \leq 0.5$</td> <td>$N \leq 4$</td> </tr> <tr> <td>$0.5 < D$</td> <td>NONE</td> </tr> <tr> <td rowspan="3">CF FAIL / SPOT</td> <td>$D \leq 0.15$</td> <td>IGNORE</td> </tr> <tr> <td>$0.15 < D \leq 0.5$</td> <td>$N \leq 4$</td> </tr> <tr> <td>$0.5 < D$</td> <td>NONE</td> </tr> </tbody> </table> <p>NOTE : (1) POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA.</p> <p>(2) THE EXTRANEIOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON.</p> <p>(3) THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING.</p> <p>AVERAGE DIAMETER (D)=(a+b)/2</p> <div style="text-align: center;">  </div>		AVERAGE DIAMETER (mm) : D	NUMBER OF PIECES PERMITTED	BUBBLE ON THE POLARIZER	$D \leq 0.15$	IGNORE	$0.15 < D \leq 0.5$	$N \leq 4$	$0.5 < D$	NONE	SURFACE STAINS	$D \leq 0.15$	IGNORE	$0.15 < D \leq 0.5$	$N \leq 4$	$0.5 < D$	NONE	CF FAIL / SPOT	$D \leq 0.15$	IGNORE	$0.15 < D \leq 0.5$	$N \leq 4$	$0.5 < D$	NONE
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NO.	ITEM	CRITERIA												
5	BLACK/WHITE SPOT CIRCULAR TYPE	THE FOLLOWING BLACK/WHITE SPOT ARE WITHIN THE VIEWING AREA. AVERAGE DIAMETER : D (mm) <table border="1"> <thead> <tr> <th>SIZE D</th> <th>PERMISSIBLE NO.</th> </tr> </thead> <tbody> <tr> <td>$D \leq 0.3$</td> <td>IGNORE</td> </tr> <tr> <td>$0.3 < D \leq 0.5$</td> <td>5</td> </tr> <tr> <td>$D > 0.5$</td> <td>0</td> </tr> </tbody> </table> NOTE (1) : THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.		SIZE D	PERMISSIBLE NO.	$D \leq 0.3$	IGNORE	$0.3 < D \leq 0.5$	5	$D > 0.5$	0			
SIZE D	PERMISSIBLE NO.													
$D \leq 0.3$	IGNORE													
$0.3 < D \leq 0.5$	5													
$D > 0.5$	0													
6	SCRATCH	THE FOLLOWING SCRATCH IS WITHIN THE VIEWING AREA. WIDTH : W (mm) , LENGTH : L (mm) <table border="1"> <thead> <tr> <th>SIZE W & L</th> <th>PERMISSIBLE NO.</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.15$</td> <td>IGNORE</td> </tr> <tr> <td>$0.15 < W \leq 0.2, L \leq 8$</td> <td>5</td> </tr> <tr> <td>$W > 0.2$</td> <td>0</td> </tr> </tbody> </table> NOTE (1) : THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.		SIZE W & L	PERMISSIBLE NO.	$W \leq 0.15$	IGNORE	$0.15 < W \leq 0.2, L \leq 8$	5	$W > 0.2$	0			
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$W \leq 0.15$	IGNORE													
$0.15 < W \leq 0.2, L \leq 8$	5													
$W > 0.2$	0													
7	BLACK / WHITE LINE LINEAR TYPE / FOREIGN FIBER	THE FOLLOWING BLACK LINE, WHITE LINE IS WITHIN THE VIEWING AREA. WIDTH : W (mm) , LENGTH : L (mm) <table border="1"> <thead> <tr> <th>SIZE W & L</th> <th>PERMISSIBLE NO.</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.15$</td> <td>IGNORE</td> </tr> <tr> <td>$0.15 < W \leq 0.2, L \leq 8$</td> <td>5</td> </tr> <tr> <td>$W > 0.2$</td> <td>0</td> </tr> </tbody> </table> NOTE (1) : THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.		SIZE W & L	PERMISSIBLE NO.	$W \leq 0.15$	IGNORE	$0.15 < W \leq 0.2, L \leq 8$	5	$W > 0.2$	0			
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8	BUBBLE / DENT FOR OPTICAL BONDING	BUBBLES WITHIN VIEWING AREA. AVERAGE DIAMETER : D (mm) <table border="1"> <thead> <tr> <th>SIZE D</th> <th>PERMISSIBLE NO.</th> </tr> </thead> <tbody> <tr> <td>$D \leq 0.2$</td> <td>IGNORE</td> </tr> <tr> <td>$0.2 < D \leq 0.3$</td> <td>3</td> </tr> <tr> <td>$0.3 < D \leq 0.5$</td> <td>2</td> </tr> <tr> <td>$D > 0.5$</td> <td>0</td> </tr> </tbody> </table> NOTE (1) : THE DISTANCE BETWEEN DEFECTS SHOULD BE MORE THAN 10mm APART.		SIZE D	PERMISSIBLE NO.	$D \leq 0.2$	IGNORE	$0.2 < D \leq 0.3$	3	$0.3 < D \leq 0.5$	2	$D > 0.5$	0	
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9	CHIPPING	<table border="1"> <tr> <td>CORNER</td> <td>$X \leq 3\text{mm} \cdot Y \leq 3\text{mm} \cdot Z \leq t$ (t : THICKNESS)</td> </tr> <tr> <td>EDGE</td> <td>$X \leq 6\text{mm} , Y \leq 1\text{mm} , Z < t$ (t : THICKNESS)</td> </tr> </table>	CORNER	$X \leq 3\text{mm} \cdot Y \leq 3\text{mm} \cdot Z \leq t$ (t : THICKNESS)	EDGE	$X \leq 6\text{mm} , Y \leq 1\text{mm} , Z < t$ (t : THICKNESS)								
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EDGE	$X \leq 6\text{mm} , Y \leq 1\text{mm} , Z < t$ (t : THICKNESS)													
10	CRACKED GLASS	NOT ACCEPTABLE												
11	LINE DEFECT ON DISPLAY	OBVIOUS VERTICAL OR HORIZONTAL LINE DEFECT IS NOT ALLOWED.												
12	MURA & LEAK ON DISPLAY	IT'S ACCEPTABLE, IF MURA AND LEAK IS SLIGHT VISIBLE THROUGH 5% ND FILTER.												
13	UNEVEN COLOR SPREAD, COLORATION	TO BE DETERMINED BASED UPON THE LIMITED SAMPLE.												
14	BEZEL APPEARANCE	1. BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS OF OTHER CONTAMINATION. 2. BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.												

NO.	ITEM	CRITERIA
15	PCB	<ol style="list-style-type: none"> 1. THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES. 2. NO OXIDATION OR CONTAMINATION ON PCB TERMINALS. 3. PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART. THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS. 4. THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART. 5. IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD; MAKE SURE IT IS SMOOTHED DOWN.
16	SOLDERING	<ol style="list-style-type: none"> 1. NO SOLDERING FOUND ON THE SPECIFIED PLACE 2. INSUFFICIENT SOLDER <ol style="list-style-type: none"> (a) LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR "HEEL" OF LEAD AND PAD  (b) CHIP COMPONENT <ul style="list-style-type: none"> · SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING  · SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  3. PARTS ALIGNMENT <ol style="list-style-type: none"> (a) LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE  (b) CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  4. NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. 5. NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. 6. NO RESIDUE OR SOLDER BALLS ON PCB. 7. NO SHORT CIRCUITS IN COMPONENTS ON PCB.

NO.	ITEM	CRITERIA
17	BACKLIGHT	<ol style="list-style-type: none"> 1. NO LIGHT 2. FLICKERING AND OTHER ABNORMAL ILLUMINATION 3. SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. 4. BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.
18	GENERAL APPEARANCE	<ol style="list-style-type: none"> 1. NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. 2. NO CRACKS ON INTERFACE PIN (OLB) OF TCP. 3. NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. 4. THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. 5. THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. 6. THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. 7. SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. 8. PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. 9. LCD PIN LOOSE OR MISSING PINS. 10. PRODUCT PACKAGING MUST BE THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. 11. PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. 12. THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

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14 RELIABILITY TEST

14.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO.	ITEM	DESCRIPTION
1	HIGH TEMPERATURE TEST (OPERATION)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +70°C FOR 240 HRS
2	LOW TEMPERATURE TEST (OPERATION)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -20°C FOR 240 HRS
3	HIGH TEMPERATURE TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT +80°C FOR 240 HRS
4	LOW TEMPERATURE TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT -30°C FOR 240 HRS
5	HIGH TEMPERATURE / HUMIDITY TEST (STORAGE)	THE SAMPLE SHOULD BE ALLOWED TO STAND AT 60°C, 90% RH 240 HRS
6	THERMAL SHOCK TEST (NOT OPERATED)	<p>THE SAMPLE SHOULD BE ALLOWED TO STAND THE FOLLOWING 10 CYCLES OF OPERATION :</p>
7	VIBRATION (NOT OPERATED)	11.76 m/s ² (1.2G), 10~100 Hz XYZ DIRECTIONS, 1 HR EACH
8	SHOCK (NOT OPERATED)	490.0 m/s ² (50G), 10 ms XYZ DIRECTIONS, 1 TIME EACH
9	ESD (ELECTROSTATIC DISCHARGE) (NOT OPERATED)	AIR DISCHARGE ± 12KV CONTACT DISCHARGE ± 8KV (ACCORDING TO IEC-61000-4-2)

NOTE (1) : THE TEST SAMPLES HAVE RECOVERY TIME FOR 2 HOURS AT ROOM TEMPERATURE BEFORE THE FUNCTION CHECK. IN THE STANDARD CONDITIONS, THERE IS NO DISPLAY FUNCTION NG ISSUE OCCURRED.

NOTE (2) : WHEN THE LCD MODULE IS OPERATED AT A HIGHER AMBIENT TEMPERATURE THAN 60°C, THE PWM DUTY CYCLE OF THE LED BACKLIGHT SHOULD BE ADJUSTED TO BE LESS THAN TBD%. IF THE MODULE IS OPERATED AT A HIGHER DUTY CYCLE THAN TBD, THEN THERE IS A POSSIBILITY OF DISTORTION AND IRREGULARITY OF THE PICTURE DUE TO LIQUID CRYSTAL BEHAVIOR.

NOTE (3) : TESTING CONDITIONS AND INSPECTION CRITERIA

NO.	ITEM	TEST MODEL	INSPECTION CRITERIA
1	CURRENT CONSUMPTION	REFER TO SPECIFICATION	THE CURRENT CONSUMPTION SHOULD CONFORM TO THE PRODUCT SPECIFICATION.
2	CONTRAST	REFER TO SPECIFICATION	AFTER THE TESTS HAVE BEEN EXECUTED, THE CONTRAST MUST BE LARGER THAN HALF OF ITS INITIAL VALUE PRIOR TO THE TESTS.
3	APPEARANCE	VISUAL INSPECTION	DEFECT FREE

15. CAUTION

15.1 OPERATION

15.1.1 DO NOT CONNECT OR DISCONNECT MODULES TO OR FROM THE MAIN SYSTEM WHILE POWER IS BEING SUPPLIED .

15.1.2 USE THE MODULE WITHIN SPECIFIED TEMPERATURE ; LOWER TEMPERATURE CAUSES THE RETARDATION OF BLINKING SPEED OF THE DISPLAY ; HIGHER TEMPERATURE MAKES OVERALL DISPLAY DISCOLOR.

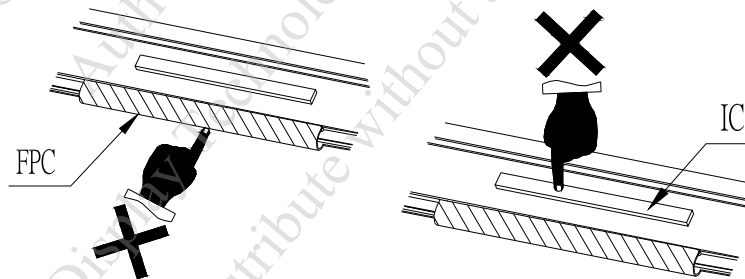
WHEN THE TEMPERATURE RETURNS TO NORMALITY, THE DISPLAY WILL OPERATE NORMALLY .

15.1.3 ADJUST THE LC DRIVING VOLTAGE TO OBTAIN THE OPTIMUM CONTRAST.

15.1.4 POWER ON SEQUENCE INPUT SIGNALS SHOULD NOT BE SUPPLIED TO LCD MODULE BEFORE POWER SUPPLY VOLTAGE IS APPLIED AND REACHES THE SPECIFIED VALUE .

IF ABOVE SEQUENCE IS NOT FOLLOWED , CMOS LSIS OF LCD MODULES MAY BE DAMAGED DUE TO LATCH - UP PROBLEM .

15.1.5 NOT ALLOWED TO INFLICT ANY EXTERNAL STRESS AND TO CAUSE ANY MECHANICAL INTERFERENCE ON THE BENDING AREA OF FPC DURING THE TAIL BENDING BACKWARDS!
DO NOT STRESS FPC AND IC ON THE MODULE!



15.2 NOTICE

- 15.2.1 USE A GROUNDED SOLDERING IRON WHEN SOLDERING CONNECTOR I/O TERMINALS . FOR SOLDERING OR REPAIRING, TAKE PRECAUTION AGAINST THE TEMPERATURE OF THE SOLDERING IRON AND THE SOLDERING TIME TO PREVENT PEELING OFF THE THROUGH-HOLE-PAD .
- 15.2.2 DO NOT DISASSEMBLE . EDT SHALL NOT BE HELD RESPONSIBLE IF THE MODULE IS DISASSEMBLED AND UPON THE REASSEMBLY THE MODULE FAILED .
- 15.2.3 DO NOT CHARGE STATIC ELECTRICITY , AS THE CIRCUIT OF THIS MODULE CONTAINS CMOS LSIS. A WORKMAN'S BODY SHOULD ALWAYS BE STATIC-PROTECTED BY USE OF AN ESD STRAP. WORKING CLOTHES FOR SUCH PERSONNEL SHOULD BE OF STATIC-PROTECTED MATERIAL.
- 15.2.4 ALWAYS GROUND THE ELECTRICALLY-POWERED DRIVER BEFORE USING IT TO INSTALL THE LCD MODULE. WHILE CLEANING THE WORK STATION BY VACUUM CLEANER, DO NOT BRING THE SUCKING MOUTH NEAR THE MODULE ; STATIC ELECTRICITY OF THE ELECTRICALLY-POWERED DRIVER OR THE VACUUM CLEANER MAY DESTROY THE MODULE .
- 15.2.5 DON'T GIVE EXTERNAL SHOCK.
- 15.2.6 DON'T APPLY EXCESSIVE FORCE ON THE SURFACE.
- 15.2.7 LIQUID IN LCD IS HAZARDOUS SUBSTANCE. MUST NOT LICK AND SWALLOW.
WHEN THE LIQUID IS ATTACH TO YOUR, SKIN, CLOTH ETC.
WASH IT OUT THOROUGHLY AND IMMEDIATELY.
- 15.2.8 DON'T OPERATE IT ABOVE THE ABSOLUTE MAXIMUM RATING.
- 15.2.9 STORAGE IN A CLEAN ENVIRONMENT, FREE FROM DUST, ACTIVE GAS AND SOLVENT.
- 15.2.10 STORE WITHOUT ANY PHYSICAL LOAD.
- 15.2.11 REWIRING: NO MORE THAN 3 TIMES.

15.3 STORAGE

- (1)STORE THE MODULE IN A DARK ROOM OR KEEP IN ORIGINAL PACKAGE WHERE MUST KEEP AT $25\pm 10^{\circ}\text{C}$ AND 65%RH OR LESS.
- (2)DO NOT STORE THE MODULE IN SURROUNDINGS CONTAINING ORGANIC SOLVENT OR CORROSIVE GAS.
- (3)STORE THE MODULE IN AN ANTI-ELECTROSTATIC CONTAINER OR BAG.