Datasheet

60 Series SOM

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	13 Nov 2018	Initial Version	Andrew Chen	Jay White

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CONTENTS

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1 SCOPE

This document describes key hardware aspects of the Laird 60 Series system on module (SOM). This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from many sources and includes information found in the Laird 60-SIPT, Marvell 88W8997/88PG823, and Atmel/Microchip ATSAMA5D3X.

Note that the information in this document is subject to change. Please contact Laird to obtain the most recent version of this document.

2 INTRODUCTION

2.1 General Description

The Laird 60 Series SOM wireless bridge module is a wireless communications subsystem that may be integrated into a variety of host devices via many available electronic and logical interfaces. The SOM provides complete enterprise-class Wi-Fi connectivity with an integrated TCP/IP stack. It also provides full support for 2x2 MIMO 802.11 a/b/g/n/ac WLAN plus Bluetooth 4.2 dual mode dual-mode air standards with a fully integrated security supplicant providing 802.11i/WPA2 Enterprise authentication, data encryption, and BT protocol stacks.

The 60 SOM has a wide variety of interfaces including RMII, RGMII, serial UART, Hi-Speed USB, SPI, SDIO, TTL RGB, PCM, and I2C. The wireless bridge may be configured, monitored, and managed via a Command Line Interface (CLI) over an available dedicated console port, via a web interface over a wireless or Ethernet interface, or via a remote SDK interface over wireless or Ethernet.

The 60 SOM incorporates the Laird 60-SIPT Wi-Fi SiP module which uses Marvell 88W8997/88PG823. The product also features a Cortex A5 processor running at 536 MHz and a MCP memory with 1 Gb 32-bits of Lower Power DDR (LPDDR) memory, and 2 Gb 8-bits of SLC NAND flash storage. Several GPIO lines are available for data acquisition and similar applications. The platform should support the Linux OS version 3.0.x to current highest LTS version. A software developer's kit (SDK) with Application Programming Interfaces (API) and software tools are available for the development of custom software applications on the device.

2.2 Features and Functionality

The 60 SOM is based on the ATSAMA5D36 processor from Atmel/Microchip. This processor offers several interfaces, some of which are multiplexed and not available simultaneously. The module has the following features:

- ATSAMA5D34 single ARM Cortex-A5 core operating at speeds up to 536 MHz:
  - 32-Kb L1 instruction cache
  - 32-Kbyte data cache, 32-Kbyte instruction cache, Virtual Memory System Architecture (VMSA)
  - 160-Kbyte internal ROM single-cycle access at system speed.
  - One 128-Kbyte internal SRAM, single-cycle access at system speed
  - Very slow clock operating mode, software programmable power optimization capabilities
- Security:
  - TRNG: True random number generator
  - AES: 256-bit, 192-bit, 128-bit key algorithm, compliant with FIPS PUB 197 Specifications
  - TDES: Two-key or three-key algorithms, compliant with FIPS PUB 46-3 Specifications
  - Atmel/Microchip secure boot solution
- Memory:
  - 1 Gb, 32-bits of Lower Power DDR (LPDDR) memory
  - 2 Gb, 8-bits of SLC NAND flash memory
- 2X2 IEEE 802.11 a/b/g/n/ac WLAN interface
- Bluetooth version 4.2 dual-mode
- Support interface:
  - 24-bits TTL RGB bus for TFT LCD display
  - X1 MMC/SD/SDIO card port

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  - X3 HS/FS/LS USB Ports with: X1 USB device port. X2 USB host ports.
  - X1 10/100/1000 Mbps reduced Gigabit media independent interface (RGMII)
  - X1 10/100 Mbps reduced media-independent interface (RMII)
  - X1 CAN bus, fully compliant with CAN 2.0 Part A and 2.0 Part B
  - X3 UARTs
  - X1 DBGU for debug purpose
  - X2 Master/Slave serial peripheral interfaces
  - X1 Synchronous serial controllers
  - X2 Two-wire interface up to 400 Kbit/s supporting I2C Protocol and SMBUS
  - ADC and GPIOs
- Ultra-miniature low profile SMT module (30 x 30 x 2.8 mm) based on 188 pads 2 row LGA package

The 60 SOM provides the following two U. FL type antenna connectors that provide two streams MIMO operation to reach the maximum data rate:

- Main/ANT0 antenna – Wi-Fi only
- Auxiliary/ANT1 – Wi-Fi and Bluetooth

Bluetooth signals can only be presented at the auxiliary/ANT1. Supported host device antenna types include dipole and monopole antennas.

Regulatory operational requirements are included in this document and may be incorporated into the operating manual of any device into which the 60 SOM is installed. The 60 SOM is designed for installation into mobile devices which typically operate at distances greater than 20 cm from the human body and portable devices which typically operate at distances less than 20 cm from the human body. See Documentation Requirements for more information.

The 60 Series SOM modules include two product SKUs which have different supported software features. Please check Laird sales/FAE for further information. Order information is listed below:

Part Number	Description
453-00003	60 Series SOM
455-00003	Development board for the 60 Series SOM
455-00004	LCD Touchscreen for the 60 Series SOM development board (add-on)

CAUTION: The 60 Series SOM only allows one time reflow during the SMT assembly process. Applying more than one time reflow during this process will damage the module.

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2.3 Block Diagram

Figure 1 show block diagrams of the Laird 60 Series SOM.

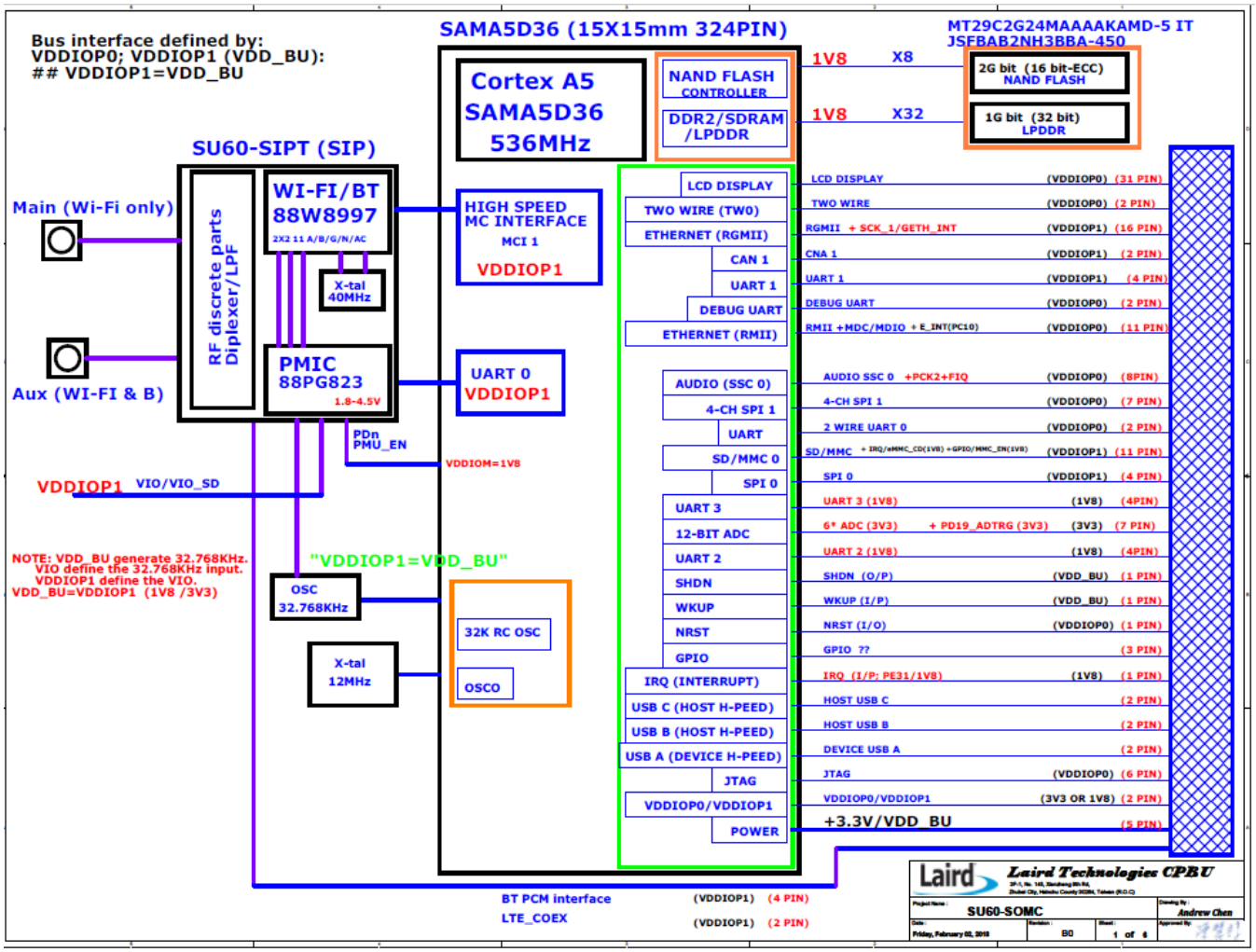

Figure 1: Laird 60 SOM module block diagrams

Note: Transmitter frequencies for Wi-Fi are 2412-2462 MHz and 5180-5805 MHz. Transmitter frequencies for Bluetooth are 2402-2480 MHz.

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3 Pin Definitions and Signal Descriptions

Note:		
	PWR	Power Input
	I/O	Input and output
	I	Input
	O	Output
	PU	Pull-up
	PD	Pull-down

Table 1: 60 SOM pin definitions

Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
G1	GND	-	-	-	Ground	GND
A1	VCC3_3	PWR	-	-	DC 3.3V input for the module	--
A2	GND	-	-	-	Ground	GND
A3	G_125CK	I	PB18	VDDIOP1	RGMII 125 MHz input clock	NC
A4	G_RXCK	I	PB11	VDDIOP1	RGMII Receive clock	NC
A5	G_RXER	I	PB13	VDDIOP1	RGMII Receive error	NC
A6	GND	-	-	-	Ground	GND
A7	G_RX3	I	PB7	VDDIOP1	RGMII Receive data	NC
A8	G_MDIO	I/O	PB17	VDDIOP1	RGMII Management data Input/Output	NC
A9	G_RX1	I	PB5	VDDIOP1	RGMII Receive data	NC
A10	G_RX0	I	PB4	VDDIOP1	RGMII Receive data	NC
A11	G_RX2	I	PB6	VDDIOP1	RGMII Receive data	NC
A12	GND	-	-	-	Ground	GND
A13	GND	-	-	-	Ground	GND
A14	G_TXCK	O	PB8	VDDIOP1	RGMII Transmit clock or Reference clock	NC
A15	G_TXEN	O	PB9	VDDIOP1	RGMII Transmit Enable	NC
A16	GND	-	-	-	Ground	GND
A17	G_TX2	O	PB2	VDDIOP1	RGMII Transmit data	NC
A18	G_TX3	O	PB3	VDDIOP1	RGMII Transmit data	NC
A19	G_TX0	O	PB0	VDDIOP1	RGMII Transmit data	NC
A20	G_TX1	O	PB1	VDDIOP1	RGMII Transmit data	NC
A21	G_MDC	O	PB16	VDDIOP1	RGMII Management data clock	NC
A22	GND	-	-	-	Ground	GND
A23	GND	-	-	-	Ground	GND
A24	TW_CLK	I/O	PA31	VDDIOP0	Two-wire Serial clock	NC
A25	TW_D	I/O	PA30	VDDIOP0	Two-wire Serial data	NC
A26	GND	-	-	-	Ground	GND

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
A27	ADTRG	I	PD19	VDDIOP1	ADC Trigger	NC
A28	AD3	I	PD23	VCC3_3	Touchscreen Analog-to-Digital Converter – ADC Lower Right touch panel	NC
A29	AD4	I	PD24	VCC3_3	Touchscreen Analog-to-Digital Converter – ADC Panel Input	NC
A30	AD0	I	PD20	VCC3_3	Touchscreen Analog-to-Digital Converter – ADC Upper-left touch panel	NC
A31	AD5	I	PD25	VCC3_3	Analog Input	NC
A32	AD1	I	PD21	VCC3_3	Touchscreen Analog-to-Digital Converter – ADC Upper-right touch panel	NC
A33	AD2	I	PD22	VCC3_3	Touchscreen Analog-to-Digital Converter – ADC Lower-left touch panel	NC
A34	GND	-	-	-	Ground	GND
A35	FIQ	I/PU	PC31	VDDIOP0	Fast Interrupt Default: Interrupt signal from Audio Codec chip.	NC
A36	GND	-		-	Ground	GND
A37	VDDIOP1	PWR	-	-	I/O Port 1 Reference Voltage; 1.8V or 3.3V	--
A38	URXD0	I	PC29	VDDIOP0	UART0 Receive data	NC
A39	UTXD0	O	PC30	VDDIOP0	UART0 Transmit data	NC
A40	GND	-	-	-	Ground	GND
A41	TK0	I/O	PC16	VDDIOP0	Synchronous Serial Controller (SSC) Transmit clock	NC
A42	TD0	O	PC18	VDDIOP0	Synchronous Serial Controller (SSC) Transmit data	NC
A43	PCK2	O	PC15	VDDIOP0	Programmable Clock Output; Default: Master clock for Audio CODEC	NC
A44	RF0	I/O	PC20	VDDIOP0	Synchronous Serial Controller (SSC) Receive Frame Sync	NC
A45	TF0	I/O	PC17	VDDIOP0	Synchronous Serial Controller (SSC) Transmit Frame Sync	NC
A46	RD0	I	PC21	VDDIOP0	Synchronous Serial Controller (SSC) Receive data	NC
A47	RK0	I/O	PC19	VDDIOP0	Synchronous Serial Controller (SSC) Receive clock	NC
G2	GND	-	-	-	Ground	GND
B1	VCC3_3	PWR	-	-	DC 3.3V input for the module	--
B2	GND	-	-	-	Ground	GND
B3	GPIO Default:	I	PC14	VDDIOP0	Device USB Bus Power Sense **H** – USB device port is plugged into a host	10k;PL

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
	VBUS_SENSE				**L** – USB device port is NOT plugged into a host	
B4	E_TXEN	O	PC4	VDDIOP0	RMII Transmit Enable	NC
B5	GPIO Default: E_INT	I	PC10	VDDIOP0	RMII Interrupt Input from Ethernet PHY	NC
B6	E_RXD1	I	PC3	VDDIOP0	RMII Receive data	NC
B7	E_MDIO	I/O	PC9	VDDIOP0	RMII Management Data Input/Output	NC
B8	E_RXD0	I	PC2	VDDIOP0	RMII Receive data	NC
B9	E_RXER	I	PC6	VDDIOP0	RMII Receive error	NC
B10	E_CRSDV	I	PC5	VDDIOP0	RMII Carrier Sense/Data Valid	NC
B11	E_MDC	O	PC8	VDDIOP0	RMII Management Data clock	NC
B12	E_TXD1	O	PC1	VDDIOP0	RMII Transmit data	NC
B13	E_TXD0	O	PC0	VDDIOP0	RMII Transmit data	NC
B14	GND	-	-	-	Ground	GND
B15	E_REFCK	I	PC7	VDDIOP0	RMII Transmit Clock or Reference clock	NC
B16	GND	-	-	-	Ground	GND
B17	SPI1_CLK	I/O	PC24	VDDIOP0	SPI1 Serial clock	NC
B18	GND	-	-	-	Ground	GND
B19	SPI1_MISO	I/O	PC22	VDDIOP0	SPI1 Master In Slave Out	NC
B20	SPI1_MOSI	I/O	PC23	VDDIOP0	SPI1 Master Out Slave In	NC
B21	SPI1_NPCS2 Default: TW_CK1	I/O	PC27	VDDIOP0	SPI1 Peripheral Chip Select TW_CK1: Two-wire Serial clock	NC
B22	GND	-	-	-	Ground	GND
B23	LCD_DAT4	O	PA4	VDDIOP0	LCD Controller (LCDC) data bus	NC
B24	LCD_DAT2	O	PA2	VDDIOP0	LCD Controller (LCDC) data bus	NC
B25	LCD_DAT14	O	PA14	VDDIOP0	LCD Controller (LCDC) data bus	NC
B26	LCD_PWM	O	PA24	VDDIOP0	LCDPWM for LCD Panel Contrast Control	NC
B27	LCD_DAT10	O	PA10	VDDIOP0	LCD Controller (LCDC) data bus	NC
B28	LCD_DAT0	O	PA0	VDDIOP0	LCD Controller (LCDC) data bus	NC
B29	LCD_DAT12	O	PA12	VDDIOP0	LCD Controller (LCDC) data bus	NC
B30	GND	-	-	-	Ground	GND
B31	LCD_PCK	O	PA28	VDDIOP0	LCD Controller (LCDC) LCD pixel clock	NC
B32	GND	-	-	-	Ground	GND
B33	LCD_DAT22	O	PA22	VDDIOP0	LCD Controller (LCDC) data bus	NC
B34	LCD_DAT20	O	PA20	VDDIOP0	LCD Controller (LCDC) data bus	NC
B35	LCD_DAT8	O	PA8	VDDIOP0	LCD Controller (LCDC) data bus	NC

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
B36	LCD_VSYNC	O	PA26	VDDIOP0	LCD Controller (LCDC) LCD vertical synchronization	NC
B37	LCD_DAT3	O	PA3	VDDIOP0	LCD Controller (LCDC) data bus	NC
B38	LCD_HSYNC	O	PA27	VDDIOP0	LCD Controller (LCDC) LCD horizontal synchronization	NC
B39	LCD_DAT16	O	PA16	VDDIOP0	LCD Controller (LCDC) data bus	NC
B40	LCD_DAT6	O	PA6	VDDIOP0	LCD Controller (LCDC) data bus	NC
B41	LCD_DAT1	O	PA1	VDDIOP0	LCD Controller (LCDC) data bus	NC
B42	LCD_DISP	O	PA25	VDDIOP0	LCD Controller (LCDC) LCD Display ON/OFF	NC
B43	LCD_DAT18	O	PA18	VDDIOP0	LCD Controller (LCDC) data bus	NC
B44	LCD_DAT15	O	PA15	VDDIOP0	LCD Controller (LCDC) data bus	NC
B45	LCD_DAT13	O	PA13	VDDIOP0	LCD Controller (LCDC) data bus	NC
B46	LCD_DAT17	O	PA17	VDDIOP0	LCD Controller (LCDC) data bus	NC
B47	LCD_DEN	O	PA29	VDDIOP0	LCD Controller (LCDC) LCD data enable	NC
G3	GND	-	-	-	Ground	GND
C1	LCD_DAT19	O	PA19	VDDIOP0	LCD Controller (LCDC) data bus	NC
C2	LCD_DAT23	O	PA23	VDDIOP0	LCD Controller (LCDC) data bus	NC
C3	LCD_DAT21	O	PA21	VDDIOP0	LCD Controller (LCDC) data bus	NC
C4	GND	-	-	-	Ground	GND
C5	SPI1_NPCS3 Default: TW_IRQ1	I/O	PC28	VDDIOP0	SPI1 Peripheral Chip Select TW_IRQ1:Two-wire interrupt Touch screen change Interrupt (I/P)	NC
C6	SPI1_NPCS1 Default: TW_D1	I/O	PC26	VDDIOP0	SPI1 Peripheral Chip Select TW_D1: Two-wire serial data	NC
C7	SPI1_NPCS0 Default: LCD_Mode	O	PC25	VDDIOP0	SPI1 Peripheral Chip Select LCD_Mode Select: **H –** DE mode; **L –** HSD/VSD mode	NC
C8	LCD_DAT7	O	PA7	VDDIOP0	LCD Controller (LCDC) data bus	NC
C9	LCD_DAT9	O	PA9	VDDIOP0	LCD Controller (LCDC) data bus	NC
C10	LCD_DAT5	O	PA5	VDDIOP0	LCD Controller (LCDC) data bus	NC
C11	LCD_DAT11	O	PA11	VDDIOP0	LCD Controller (LCDC) data bus	NC
C12	GND	-	-	-	Ground	GND
C13	GND	-	-	-	Ground	GND
C14	GND	-	-	-	Ground	GND
C15	WIFI_3V3	PWR			3.3V Power Supply for Wi-Fi SIP on the module	--
C16	LTE_SIN	I	-	VDDIOP1	LTE Coex. Signal Input	NC

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
C17	LTE_SOUT	O	-	VDDIOP1	LTE Coex. Signal Output	NC
C18	GND	-	-	-	Ground	GND
C19	GPIO Default: eMMC_Disable	I/O	PE30	1.8V	GPIO: eMMC Card slot Power Supply Control O/P:Low to disable the eMMC power	NC
C20	IRQ Default: eMMC_CD	I/O	PE31	1.8V	IRQ eMMC Card Card Detect I/P: Low Active. **L –** detect SDIO card inserted	10K;PU
C21	GND	-	-	-	Ground	GND
C22	GND	-	-	-	Ground	GND
C23	VDDIOP1	PWR	-	-	I/O Port 1 Reference Voltage; 1.8V or 3.3V	--
C24	SPI0_MISO	I/O	PD10	VDDIOP1	SPI0 Master In Slave Out	NC
C25	GND	-		-	Ground	GND
C26	SPI0_CLK	I/O	PD12	VDDIOP1	SPI0 serial clock	NC
C27	GND	-	-	-	Ground	GND
C28	SPI0_MOSI	I/O	PD11	VDDIOP1	SPI0 Master Out Slave In	NC
C29	SPI0_NPCS0	O	PD13	VDDIOP1	SPI0 Peripheral Chip Select	NC
C30	GND	-	-	-	Ground	GND
C31	GND	-	-	-	Ground	GND
C32	GND	-	-	-	Ground	GND
C33	GND	-	-	-	Ground	GND
C34	RXD_2	I	PE25	1.8V	USART2 Receive data	NC
C35	GND	-		-	Ground	GND
C36	GPIO/SCK_2 Default: INTn_IO_Ex	I/O	PE20	1.8V	General purpose I/O/USART2 Serial clock Default: Interrupt signal from I/O expander chip. I/P; “Low” active	NC
C37	RTS_2	O	PE24	1.8V	USART2 Request-to-Send	NC
C38	CTS_2	I	PE23	1.8V	USART2 Clear-to-Send	NC
C39	TXD_2	O	PE26	1.8V	USART2 Transmit data	NC
C40	GND	-	-	-	Ground	GND
C41	GND	-	-	-	Ground	GND
C42	BT_PCM_IN	I	-	VDDIOP1	Bluetooth PCM Input	NC
C43	BT_PCM_SYNC	I/O	-	VDDIOP1	Bluetooth PCM Sync	NC
C44	BT_PCM_OUT	O	-	VDDIOP1	Bluetooth PCM Output	NC
C45	BT_PCM_CLK	I/O	-	VDDIOP1	Bluetooth PCM Clock	NC
C46	GND	-	-	-	Ground	GND

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
C47	RXD_3	I	PE18	1.8V	USART3 Receive data	NC
G4	GND	-	-	-	Ground	GND
D1	CTS_3	I	PE16	1.8V	USART3 Clear-to-Send	NC
D2	GPIO SCK_3	I/O	PE15	1.8V	General purpose I/O USART3 Serial clock	NC
D3	TXD_3	O	PE19	1.8V	USART3 Transmit data	NC
D4	RTS_3	O	PE17	1.8V	USART3 Request-to-Send	NC
D5	GND	-	-	-	Ground	GND
D6	GPIO/SCK_1 Default: GETH_INT	I/O	PB25	VDDIOP1	General purpose I/O; USART1 Serial clock GETN_INT: Interrupt input from RGMII PHY; Low active	4.7K;PU
D7	RTS_1	O	PB27	VDDIOP1	USART1 Request-to-Send	NC
D8	RXD_1	I	PB28	VDDIOP1	USART1 Receive data	NC
D9	CTS_1	I	PB26	VDDIOP1	USART1 Clear-to-Send	NC
D10	TXD_1	O	PB29	VDDIOP1	USART1 Transmit data	NC
D11	SHDN	O	SHDN	VDD_BU	Shutdown Control; Use to turn off the external PMU for VCC3_3 O/P;Low Active	NC
D12	GND	-	-	-	Ground	GND
D13	GND	-	-	-	Ground	GND
D14	HHSDPC	A	HHSDPC	-	USB Host Port C High Speed Data +	NC
D15	HHSDMC	A	HHSDM C	-	USB Host Port C High Speed Data -	NC
D16	GND	-	-	-	Ground	GND
D17	GND	-	-	-	Ground	GND
D18	HHSDPB	A	HHSDPB	-	USB Host Port B High Speed Data +	NC
D19	HHSDMB	A	HHSDM B	-	USB Host Port B High Speed Data -	NC
D20	GND	-	-	-	Ground	GND
C21	HSDMA		HSDMA		USB Device Port A High-Speed Data -	NC
C22	HSDPA		HSDPA		USB Device Port A High-Speed Data +	NC
D23	GND	-	-	-	Ground	GND
D24	VDD_BU	PWR	-	-	Module Backup Power for RTC mode Note: VDD_BU need to be same Voltage level as VDDIOP1	--
D25	WKUP	I/PU	WKUP	VDD_BU	Wake-Up: Wake up Module from RTC Mode. I/P;Low Active. Has 100K pull-up in the module design	NC

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Pin #	Name	Type	Pins map to CPU	Voltage Ref.	DVK Function	If Not Used
D26	BMS	I/PU	BMS	VDDIOP0	Boot Mode Select. Has 10K pull-up in the SOM module design NC: Normal Boot from NandFlash on the module GND: Boot from External Memory	NC
D27	NRST	I	NRST	VDDIOP0	Microcontroller Reset; Low Active 10K pulled-up is needed Put the 10K Ω pulled-up resistor close to this pin. And keep the trace as short as possible and avoid noise and ESD source.	10K PU
D28	GND	-	-	-	Ground	GND
D29	D_TXD	O	PB31	VDDIOP1	Debug UART Transmit data	NC
D30	D_RXD	I	PB30	VDDIOP1	Debug UART Receive data	NC
D31	CAN_RX1	I	PB14	VDDIOP1	CAN input	NC
D32	GND	-	-	-	Ground	GND
D33	CAN_TX1	O	PB16	VDDIOP1	CAN output	NC
D34	GND	-	-	-	Ground	GND
D35	MC_DA3	I/O	PD4	VDDIOP1	High Speed Multimedia Card data	NC
D36	MC_DA5	I/O	PD6	VDDIOP1	High Speed Multimedia Card data	NC
D37	MC_DA1	I/O	PD2	VDDIOP1	High Speed Multimedia Card data	NC
D38	MC_DA7	I/O	PD8	VDDIOP1	High Speed Multimedia Card data	NC
D39	MC_DA4	I/O	PD5	VDDIOP1	High Speed Multimedia Card data	NC
D40	MC_CDA	I/O	PD0	VDDIOP1	High Speed Multimedia Card Command	NC
D41	MC_DA6	I/O	PD7	VDDIOP1	High Speed Multimedia Card data	NC
D42	GND	-	-	-	Ground	GND
D43	MC_DA0	I/O	PD1	VDDIOP1	High Speed Multimedia Card data	NC
D44	MC_CLK	I/O	PD9	VDDIOP1	High Speed Multimedia Card clock	NC
D45	MC_DA2	I/O	PD3	VDDIOP1	High Speed Multimedia Card data	NC
D46	GND	-	-	-	Ground	GND
D47	VDDIOP0	PWR	-	-	I/O Port 0 Reference Voltage; 1.8V or 3.3V	--
G5-G13	GND	-	-	-	Ground	GND

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4 Power Consideration

4.1 Power Supply

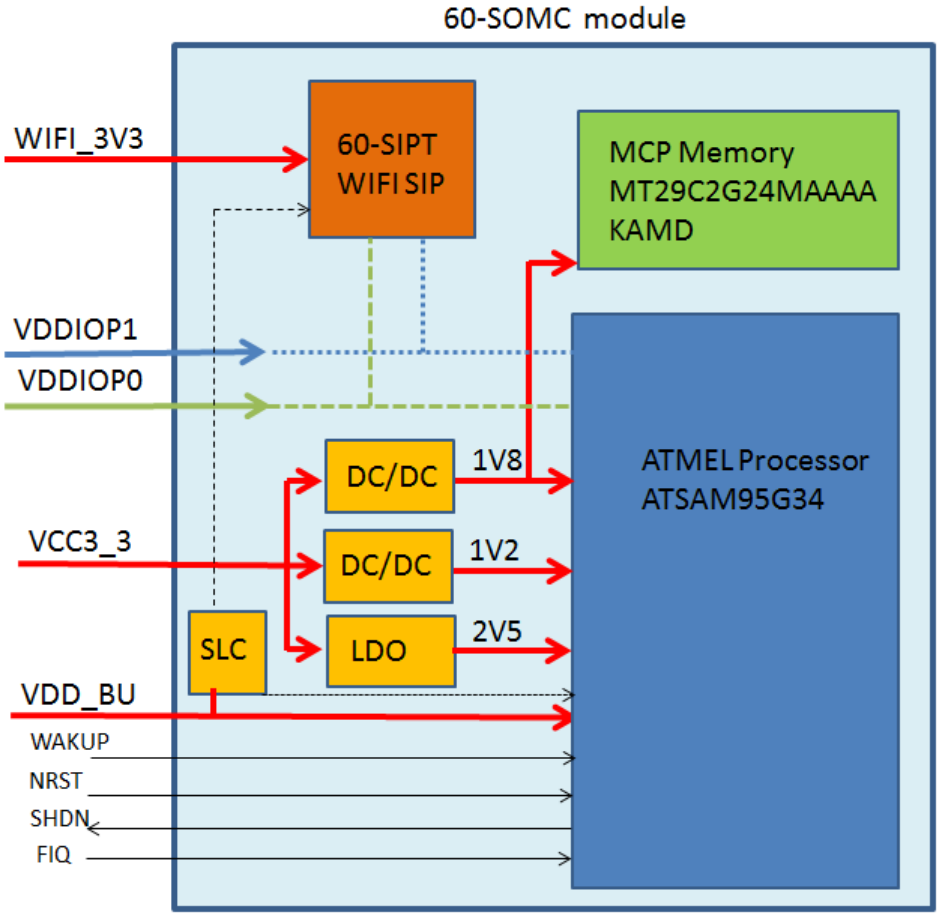

Figure 2: 60 SOM module power supply

The 60 SOM requires a primary power supply input from regulated 3.3V voltage. There are three main power rails for the module:

- WiFi_3V3 – Mainly used for the 60-SIPT Wi-Fi/BT SIP on the 60 SOM.
- VCC3_3 – Provides the input power for the processor and memory on the 60 SOM. Several DC/DC regulators and LDO generate required voltages and power on sequence (POS) timing for the processor.
- VDD_BU – Provides the backup power to the Atmel/Microchip processor on the 60 SOM. It also powers the slow clock oscillator (32.768 KHz) that provides slow clock to both the Atmel/Microchip processor and the 60-SIPT when the 60 SOM is in deep sleep mode.

The VDDIOP0 and VDDIOP1 are the Peripheral I/O's DC Supply Voltage which could be set to 1.8V or 3.3V according to the application required. Due to the VDDIOP1 defined the slow clock signal level of the 60-SIPT as well, always keep the VDD_BU and VDDIOP1 at the same voltage.

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4.2 Power on Sequence

When the power supply is connected to the 60 SOM, most of the power on sequence are designed and performed inside the 60 SOM. No specific order and timing required for the VDD_BU, VDDIOP0, VDDIOP1, WIFI_3V3, and VCC3_3. However, minimum of 5 ms (t_1) is needed for the reset (NRST) to power up.

Table 2: Power on sequence

Symbol	Parameter	Conditions	Min	Max	Unit
t_1	Reset Delay at Power-Up	From the Group established supply to NRST high	5	-	ms

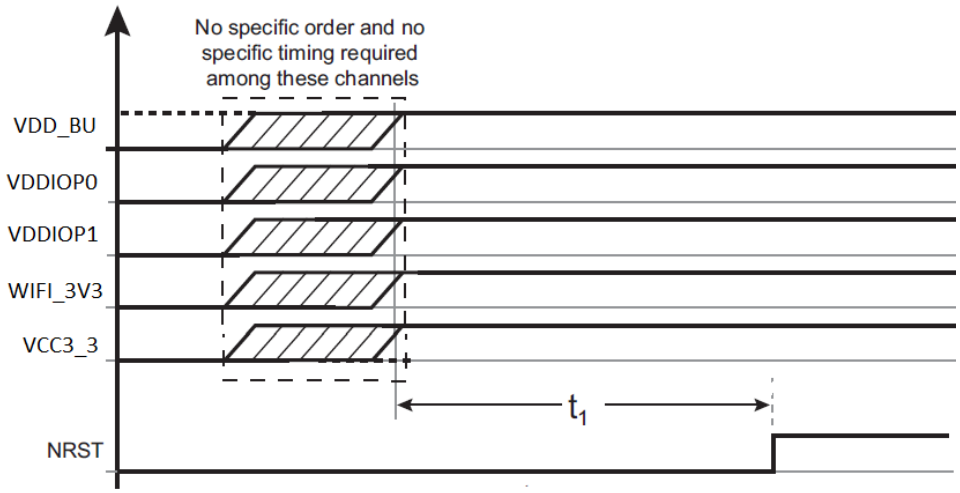

Figure 3: Power on sequence

4.3 Power Down Sequence

Table 3 provides the 60 SOM power-down sequence that starts by asserting the NRST line to 0. Once NRST is asserted, the supply inputs can be immediately shut down without any specific timing or order. Do not shut down VDD_BU if the application uses a backup battery on this supply input.

Table 3: Power down sequence

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RSTPD}	: Reset Delay at Power-Down	From NRST low to the group supply turn-off	0	-	ms

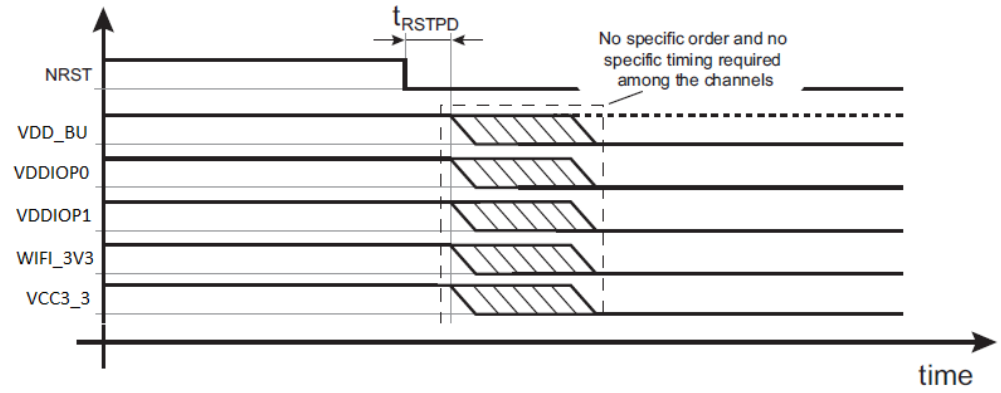

Figure 4: Power down sequence

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5 BOOTING

You can choose to boot from an external NOR Flash memory using the BMS pin. The sampling of the BMS pin is done by hardware at reset and the result is available in the BMS bit of the SFR_EBICFG register.

By default, the BMS signal is tied to high (VDDIOP0); the BMS bit is read at 1.

The ROM code standard sequence is executed, basic chip initialization and attempt to retrieve a valid code from external non-volatile memories (NVM).

Shorting points A and B together bypasses the onboard NANFlash on the 60 SOM and forces the module into ROM boot status. This allows you to program the NANDFlash through Atmel SAM-BA program.

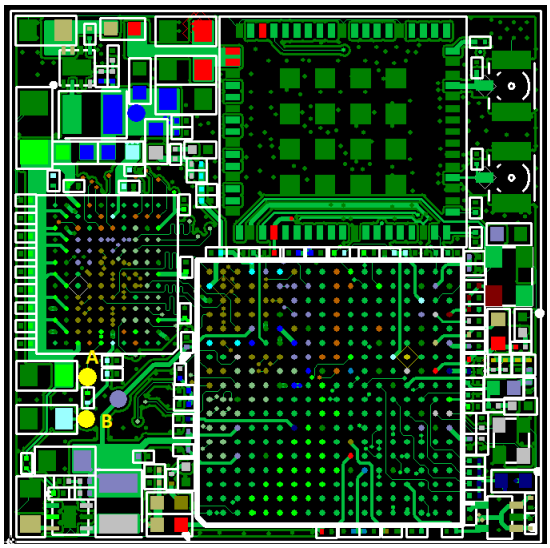

Figure 5: Shorting points A and B

If the BMS signal is tied to low, the BMS bit is read at 0.

The ROM code allows execution of the code contained in the memory connected to Chip Select 0 of the External Bus Interface.

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6 WIRELESS INTERFACE

The Laird 60 Series SOM combines a wireless local area network (WLAN) and dual-mode Bluetooth (BT) solution to support IEEE 802.11 a/b/g/n/ac 2X2 MIMO WLAN standards and BT 4.2 with the integration of WLAN/BT and Low Energy (BLE) technology.

The following sections include specifications for the wireless interfaces available on the 60 SOM.

6.1 WLAN 802.11a/b/g/n/ac

The 2.4 GHz band on the 60 SOM supports 20 MHz bandwidths and the 5 GHz band supports 20/40/80 MHz bandwidths.

The following sections specify the performance of the WLAN IEEE 802.11a/b/g/n/ac interface on the 60 SOM module.

6.1.1 WLAN RF Channels and Regulatory Domains

The 60 SOM supports the following channels and regulatory domains.

Table 4: Supported WLAN RF channels and regulatory domains

Feature	Description
Regulatory Domain Support	FCC (Americas, Parts of Asia, and Middle East) ETSI (Europe, Middle East, Africa, and Parts of Asia) IC (Industry Canada) MIC (Japan) (formerly TELEC) – Option KC (Korea) (formerly KCC) – Option
2.4 GHz Frequency Bands	**ETSI –** 2.4 GHz to 2.483 GHz **MIC –** 2.4 GHz to 2.495 GHz **FCC –** 2.4 GHz to 2.473 GHz **KC –** 2.4 GHz to 2.483 GHz
2.4 GHz Operating Channels (Wi-Fi)	**ETSI –** 13 (3 non-overlapping) **MIC –** 14 (4 non-overlapping) **FCC –** 11 (3 non-overlapping) **KC –** 13 (3 non-overlapping)
5 GHz Frequency Bands	**ETSI** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140/144) **FCC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140/144 5.725 GHz to 5.825 GHz (Ch 149/153/157/161/165) **MIC (Japan)** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140/144) **KC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124) 5.725 GHz to 5.825 GHz (Ch 149/153/157/161)
5 GHz Operating Channels (Wi-Fi)	**ETSI –** 19 non-overlapping **MIC (Japan) –** 19 non-overlapping **FCC –** 24 non-overlapping **KC –** 19 non-overlapping

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6.1.2 WLAN Modulation and Data Rate

Feature	Description
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11d, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, 802.11r, 802.11ac, 802.11w, 802.11k, 802.11v
Supported Wi-Fi Data Rates	Support 802.11 ac/a/b/g/n 2X2 MIMO 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11a/g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, HT20/HT40, MCS 0-15) 802.11ac (OFDM, HT20, MCS0-8; OFDM HT40/HT80, MCS 0-9)
Modulation	BPSK, QPSK, CCK, 16-QAM, 64-QAM, and 256-QAM. Details in the following table:

802.11ac / 802.11n	HT MCS Index	VHT MCS Index	Spatial Streams	Modulation	Coding	20 MHz		40 MHz		80 MHz	
						No SGI	SGI	No SGI	SGI	No SGI	SGI
	0	0	1	BPSK	1/2	6.5	7.2	13.5	15	29.3	32.5
	1	1	1	QPSK	1/2	13	14.4	27	30	58.5	65
	2	2	1	QPSK	3/4	19.5	21.7	40.5	45	87.8	97.5
	3	3	1	16-QAM	1/2	26	28.9	54	60	117	130
	4	4	1	16-QAM	3/4	39	43.3	81	90	175.5	195
	5	5	1	64-QAM	2/3	52	57.8	108	120	234	260
	6	6	1	64-QAM	3/4	58.5	65	121.5	135	263.3	292.5
	7	7	1	64-QAM	5/6	65	72.2	135	150	292.5	325
		8	1	256-QAM	3/4	78	86.7	162	180	351	390
		9	1	256-QAM	5/6	N/A	N/A	180	200	390	**433.3**
	8	0	2	BPSK	1/2	13	14.4	27	30	58.5	65
	9	1	2	QPSK	1/2	26	28.9	54	60	117	130
	10	2	2	QPSK	3/4	39	43.3	81	90	175.5	195
	11	3	2	16-QAM	1/2	52	57.8	108	120	234	260
	12	4	2	16-QAM	3/4	78	86.7	162	180	351	390
	13	5	2	64-QAM	2/3	104	115.6	216	240	468	520
	14	6	2	64-QAM	3/4	117	130.3	243	270	526.5	585
	15	7	2	64-QAM	5/6	130	144.4	270	300	585	650
		8	2	256-QAM	3/4	156	173.3	324	360	702	180
		9	2	256-QAM	5/6	N/A	N/A	360	400	780	**866.7**

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6.1.3 WLAN Security

Feature	Description
Security	**Standards** Wireless Equivalent Privacy (WEP) Wi-Fi Protected Access (WPA) IEEE 802.11i (WPA2) **Encryption** Wireless Equivalent Privacy (WEP, RC4 Algorithm) Temporal Key Integrity Protocol (TKIP, RC4 Algorithm) Advanced Encryption Standard (AES, Rijndael Algorithm) Encryption Key Provisioning Static (40-bit and 128-bit lengths) Pre-Shared (PSK) **Dynamic** 802.1X Extensible Authentication Protocol Types EAP-FAST, PEAP-MSCHAPv2 EAP-TLS, PEAP-TLS EAP-TTLS, LEAP PEAP-GTC

6.1.4 WLAN TX Power and RX Sensitivity

Feature	Description	
Transmit Power ***Note:*** *Transmit power on each channel varies according to individual country regulations. All values are nominal with +/-2 dBm tolerance at room temperature. Tolerance could be up to +/-2.5 dBm across operating temperature.* ***Note:*** *HT20 – 20 MHz-wide channels* *HT40 – 40 Mhz-wide channels* *HT80 – 80 MHz-wide channels*	**802.11a**	
	6 Mbps	18 dBm (63 mW)
	54 Mbps	16 dBm (40 mW)
	802.11b	
	1 Mbps	18 dBm (63 mW)
	11 Mbps	18 dBm (63 mW)
	802.11g	
	6 Mbps	18 dBm (63 mW)
	54 Mbps	16 dBm (40 mW)
	802.11n (2.4/5 GHz)	
	6.5 Mbps (MCS0-5/MCS8-13; HT20)	18 dBm (63 mW)
	65 Mbps (MCS6-7/MCS14-15; HT20)	16 dBm (40 mW)
	13.5Mbps (MCS0-5/MCS8-13; HT40)	16 dBm (40 mW)
	135Mbps (MCS6-7/MCS14-15; HT40)	14 dBm (25 mW)
	802.11ac (5 GHz)	
	6.5/13 Mbps (MCS0-6; Ntst=1,2; HT20)	18 dBm (63 mW)
	78/156 Mbps (MCS7-8; Ntst=1,2; HT20)	16 dBm (40 mW)
	13.5/27Mbps (MCS0-6; Ntst=1,2; HT40)	16 dBm (40 mW)
	180/360Mbps (MCS7-9; Ntst=1,2; HT40)	12 dBm (25 mW)
	29.3/58.5 Mbps (MCS0-5; Ntst=1,2; HT80)	14 dBm (25 mW)
	263.3/526.5 Mbps (MCS6-8; Ntst=1,2; HT80)	12 dBm (15.8 mW)
	390/780 Mbps (MCS9; Ntst=1,2; HT80)	10 dBm (10 mW)

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Feature	Description		
Typical Receiver Sensitivity (PER <= 10%) **Note:** *All values nominal, +/-3 dBm. Sensitivity on CH13/CH155 (WLAN); CH78 (BT) decades up to 4-6 dB.*	**802.11a:**		
	6 Mbps	-90 dBm	
	54 Mbps	-74 dBm	
	802.11b:		
	1 Mbps	-95 dBm	
	11 Mbps	-90 dBm	(PER<8%)
	802.11g:		
	6 Mbps	-91 dBm	
	54 Mbps	-75 dBm	
	802.11n (2.4 GHz)		
	6.5 Mbps (MCS0; HT20)	-91 dBm	
	65 Mbps (MCS7; HT20)	-73 dBm	
	13.5Mbps (MCS0; HT40)	-85 dBm	
	135Mbps (MCS7; HT40)	-70 dBm	
	802.11n (5 GHz)		
	6.5 Mbps (MCS0; HT20)	-89 dBm	
	65 Mbps (MCS7; HT20)	-70 dBm	
	13.5Mbps (MCS0; HT40)	-86 dBm	
	135Mbps (MCS7; HT40)	-69 dBm	
	802.11ac (5 GHz)		
	6.5 Mbps (MCS0; HT20)	-89 dBm	
	78 Mbps (MCS8; HT20)	-67 dBm	
	13.5 Mbps (MCS0; HT40)	-86 dBm	
	180 Mbps (MCS9; HT40)	-63 dBm	
	29.3 Mbps (MCS0; HT80)	-81 dBm	
	390/780 Mbps (MCS9; HT80)	-55 dBm	

6.2 Bluetooth

The 60 Series SOM includes a fully-integrated Bluetooth baseband/radio. Several features and functions are listed in Table 5.

Table 5: Bluetooth functions

Feature	Description
Bluetooth Interface	▪ Voice interface: – Hardware support for continual PCM data transmission/reception without processor overhead – Standard PCM clock rates from 64 kHz to 2.048 MHz with multi-slot handshake and synchronization – A-law, U-law, and linear voice PCM encoding/decoding ▪ High-speed UART interface
Bluetooth Core Functionality	▪ Bluetooth 4.2 ▪ Bluetooth Class 2/Bluetooth class 1 ▪ WLAN and Bluetooth share same LNA and antenna ▪ Digital audio interfaces with PCM/TDM interface for voice application ▪ Baseband and radio BDR and EDR package type: 1 Mbps, 2 Mbps, 3 Mbps ▪ Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correction, CRC, encryption bit stream generation, and whitening ▪ Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER) ▪ Interlaced scan for faster connection setup ▪ Simultaneous active ACL connection setup

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Feature	Description
	▪ Automatic ACL package type selection ▪ Full master and slave piconet support ▪ Scatter net support ▪ SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement ▪ All standard SCO/eSCO voice coding ▪ All standard pairing, authentication, link key, and encryption operations ▪ Encryption (AES) support
BLE Core Functionality	▪ Advertiser, scanner, initiator, master, and slave roles support (connects up to 16 links) ▪ WLAN/Bluetooth coexistence (BCA) protocol support ▪ Shared RF with BDR/EDR ▪ Encryption (AES) support ▪ Intelligent Adaptive Frequency Hopping (AFH) ▪ LE privacy 1.2 ▪ LE secure connection ▪ LE data length extension ▪ LE advertising length extension ▪ 2vMbps LE

6.2.1 Bluetooth Specification

Feature	Description
Bluetooth Media	Frequency Hopping Spread Spectrum (FHSS)
Bluetooth Standards	*Bluetooth* version 2.1 with Enhanced Data Rate *Bluetooth* 4.2 (Bluetooth Low Energy or BLE)
Supported Bluetooth Data Rates	1, 2, 3 Mbps
Bluetooth Modulation	GFSK@ 1 Mbps Pi/4-DQPSK@ 2 Mbps 8-DPSK@ 3 Mbps
Regulatory Domain Support	FCC (Americas, Parts of Asia, and Middle East) ETSI (Europe, Middle East, Africa, and Parts of Asia) IC (Industry Canada) MIC (Japan) (formerly TELEC) – Option KC (Korea) (formerly KCC) – Option
2.4 GHz Frequency Bands	2.4 GHz to 2.483 GHz
Transmit Power ***Note:*** *Transmit power on each channel varies according to individual country regulations. All values are nominal with +/-2 dBm tolerance at room temperature. Tolerance could be up to +/-2.5 dBm across operating temperature.*	**Bluetooth** 1 Mbps (1DH5) 10 dBm (12.5 mW) 2 Mbps 7 dBm (6.3 mW) 3 Mbps 7 dBm (6.3 mW) BLE (1 Mbps) 7 dBm (6.3 mW)
Typical Receiver Sensitivity (PER <= 10%) ***Note:*** *All values nominal, +/-3 dBm.*	**Bluetooth:** 1 Mbps (1DH5) -95 dBm

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Feature	Description	
Note: *Sensitivity on CH13 (WLAN)/CH78 (BT) will decade up to 4-6dB.*	2 Mbps (2DH5)	-94 dBm
	3 Mbps (3DH5)	-88 dBm
	BLE	-95 dBm

7 Module Specification

Feature	Description
Physical Interface	Two-row LGA SMD type with 1.0 mm pin pitch
Ethernet Interface	X1, 10/100 Mbps Reduced Media Independent Interface (RMII) X1, 10/100/1000 Mbps Reduced Gigabit Media Independent Interface (RGMII)
Asynchronous Serial Port Interfaces	X3, Four-wire UART with hardware handshaking (up to 921,600 baud) ***Note:*** *UART2/UART3 are for 1.8V only.*
SPI Interface	X2, master and slave modes supported with multiple chip select pins
CAN bus	X1, CAN bus, fully compliant with CAN 2.0 Part A and 2.0 Part B
USB Interfaces	X1, USB device port with high speed/full speed/low speed data rates X2, USB host ports with high speed/full speed/low speed data rates
SD/eMMC interface	X1, High-speed multimedia card data
Two Wire Interface	X1, Two-wire I2C The other two-wire interface is multiplexed with SPI bus
Debug Interface	X1, Two-wire UART (console) for debug purpose
Digital GPIO	X6, Digital General Purpose I/O (GPIO)
Analog-to-Digital Converter – ADC	X6, Analog-to-Digital converter for touch panel
Audio interface	X1, Synchronous Serial Controller (SSC)
Video interface	X1, 24-bits TTL RGB LCD display interface
PCM interface	13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats for Bluetooth
Antenna Interface	Two Hirose U.FL connectors for Wi-Fi (Main/AUX) and BT (AUX only) separately, 50 ohm
Wi-Fi Interface	Marvell 88W8997 2x2 802.11a/b/g/n/ac on 20/40/80 MHz bandwidth
Bluetooth Interface	Marvell 88W8997Bluetooth 4.2 dual-mode (EDR+BLE)
Processor Chip Set	Atmel 536 MHz ARM 9, P/N ATSAMA5D34A
Operating System	Embedded Linux, 4.1 kernel
Memory	128 MB (1 Gb) LPDDR
Storage	256 MB (2Gb) SLC NAND flash
Input Voltage Requirements	VDD_BU;VDDIOP0; VDDIOP1: 3.3V+/-10% or 1.8V+/-0.15V VCC3_3;WIFI_3V3: 3.3V+/-10% **Note**: Keep regulated voltage ripple less than 30 mV.
Operating Temperature	-30° to +85°C (-22°F to 185°F)

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Feature	Description
Operating Humidity	10 to 90% (non-condensing)
Storage Temperature	-40° to 85°C (-40° to 185°F)
Storage Humidity	10 to 90% (non-condensing)
Maximum Electrostatic Discharge	Conductive 8KV; Air coupled 12 KV follow EN61000-4-2
Size	30 mm (length) x 30 mm (width) x 2.8 mm (thickness)
Weight	5.0 g
Operating Systems Supported	Linux 3.x to 4.9.x kernel
Security	**Standards** Wireless Equivalent Privacy (WEP) Wi-Fi Protected Access (WPA) IEEE 802.11i (WPA2) **Encryption** Wireless Equivalent Privacy (WEP, RC4 Algorithm) Temporal Key Integrity Protocol (TKIP, RC4 Algorithm) Advanced Encryption Standard (AES, Rijndael Algorithm) Encryption Key Provisioning Static (40-bit and 128-bit lengths) Pre-Shared (PSK) **Dynamic** 802.1X Extensible Authentication Protocol Types EAP-FAST, PEAP-MSCHAPv2 EAP-TLS, PEAP-TLS EAP-TTLS, LEAP PEAP-GTC
Compliance	**ETSI Regulatory Domain** EN 300 328 v 2.1.1 EN 301 489-1 EN 301 489-17 EN 301 893 EN 60950-1 EU 2002/95/EC (RoHS) **FCC Regulatory Domain** FCC 15.247 DTS – 802.11b/g (Wi-Fi) – 2.4 GHz FCC 15.407 UNII – 802.11a (Wi-Fi) – 5 GHz FCC 15.247 DSS – BT 2.1 **Industry Canada** RSS-247 – 802.11a/b/g/n (Wi-Fi) – 2.4 GHz, 5.8 GHz, 5.2 GHz, and 5.4 GHz RSS-247 – BT 2.1

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Feature	Description
Certifications	**Wi-Fi Alliance** 802.11a, 802.11b, 802.11g , 802.11n, 802.11ac WPA Enterprise WPA2 Enterprise *Bluetooth*® SIG Qualification
Warranty	Three Year Warranty
All specifications are subject to change without notice	

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Table 6 summarizes the absolute maximum ratings and Table 7 lists the recommended operating conditions for the 60 SOM. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 6: Absolute maximum ratings

Symbol (Domain)	Parameter	Max Rating	Unit
VCC3_3	DC 3.3V input for the module	4.0	V
WIFI_3V3	3.3V Power Supply for Wi-Fi SIP on the module (for 1.8V system) (for 3.3V system)	4.0	V
VDD_BU	Backup Power for RTC mode	4.0	V
VDDIOP0 VDDIOP1	I/O configuration power supply (for 1.8V system) (for 3.3V system)	2.2 4.0	V
Storage	Storage Temperature	-40 to +85	°C
Voltage on Input Pins	With respect to Ground	VDDIO+0.3 (4.0 max)	V
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	+10	dBm

8.2 Recommended Operating Conditions

Table 7: Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VCC3_3; WIFI_3V3	External 3.3V power supply	3.0	3.30	3.6	V
VDD_BU; VDDIOP0; VDDIOP1	Backup and I/O configuration power supply	1.65/3.0	1.8/3.3	1.95/3.6	V
T-ambient	Ambient temperature	-30	25	85	°C

8.3 DC Electrical Characteristics

Table 8 lists the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

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Table 8: General DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Input Low-level Voltage	VDDIOPx in 3.3V range	-0.3	-	0.8	V
		VDDIOPx in 1.8V range	-0.3	-	0.54	
VIH	Input High-level Voltage	VDDIOPx in 3.3V range	2.4	-	3.6	V
		VDDIOPx in 1.8V range	1.26	-	2.1	
Vhys	Schmitt trigger Hysteresis	VDDIOPx in 3.3V range	0.34	-	-	V
		VDDIOPx in 1.8V range	0.21	-	-	
VOL	Output Low-level Voltage	IO Max	-	-	0.4	V
VOH	Output High-level Voltage	IO Max	VDDIOP-0.4	-	-	V
RPULL	Pull-up/Pull-down Resistance	VDDIOPx in 3.3V range	45	70	130	kΩ
		VDDIOPx in 1.8V range	100	160	310	
IO	Output Current	VDDIOPx in 3.3V range	8 (LO_DRIVE)	26 (ME_DRIVE)	38 (HI_DRIVE)	mA
		VDDIOPx in 1.8V range	5 (LO_DRIVE)	16 (ME_DRIVE)	22 (HI_DRIVE)	
		SCK_1/GETH_INT;	3 (LO_DRIVE)	6 (ME_DRIVE)	7 (HI_DRIVE)	
RS	Series Resistor	VBUS_SENSE	-	30	-	Ω
		SCK_1/GETH_INT	-	13	-	

8.4 Power Consumption

Table 9 and Table 10 show the power consumption of the 60 SOM when transmitting in 2.4 GHz and 5 GHz modes.

Table 9: WLAN transmitter characteristics for 2.4 GHz per chain operation

Freq.	Mode/Rate (Mbps)	Output Power Per Chain (dBm)	Typical Current Consumption Single Chain (mA)[8]	Max. Current Consumption Single Chain (mA)[8]
2417 MHz	1 Mbps	18 dBm	550	1050
	54 Mbps	16 dBm	450	820
	HT20 MCS7	16 dBm	450	820
2442 MHz	1 Mbps	18 dBm	550	1050
	54 Mbps	16 dBm	460	820
	HT20 MCS7	16 dBm	350	820
2467n MHz	1 Mbps	18 dBm	550	1050
	54 Mbps	16 dBm	450	820
	HT20 MCS7	16 dBm	450	820

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Table 10: WLAN current consumption on 5 GHz

Freq.	Mode/Rate [Mbps]	Output Power Per Chain [dBm]	Typical Current Consumption Single Chain (mA)	Typical Current Consumption Dual Chain (mA)
5200 MHz	6 Mbps	18 dBm	580	1100
	54 Mbps	16 dBm	520	970
	HT20 MCS0	18 dBm	580	1100
	HT20 MCS7	16 dBm	520	970
5190 MHz	HT40 MCS7	14 dBm	450	820
5600 MHz	6 Mbps	18 dBm	600	1200
	54 Mbps	16 dBm	530	970
	HT20 MCS0	18 dBm	600	1200
	HT20 MCS7	16 dBm	530	970
5510 MHz	HT40 MCS7	14 dBm	460	830
5825 MHz	6 Mbps	18 dBm	590	1150
	54 Mbps	16 dBm	520	980
	HT20 MCS0	18 dBm	600	1150
	HT20 MCS7	16 dBm	510	1020
5795 MHz	HT40 MCS7	14 dBm	450	850

Note: Final TX power values on each channel are limited by the regulatory certification test limit.

9 Interface Specifications

9.1 Ethernet

There are two Ethernet interfaces available on the 60 SOM that support RMII (10/100) and RGMII (10/100/1000) to comply with IEEE Standard 802.3.

9.2 Display Interface LCD

The LCD interface on 60 SOM transfers the LCD image data to an LCD display module. The LCD is programmable on a per overlay basis and supports different LCD resolutions, window sizes, image formats, and pixel depths. The following is a list of features:

- Dual AHB master interface
- Supports Single Scan Active TFT display
- Supports 12-, 16-, 18-, and 24-bit output mode through the spatial dithering unit
- Supports asynchronous output mode (at synthesis time)
- 1, 2, 4, 8 bits per pixel (palletized)
- 12, 16, 18, 19, 24, 25, and 32 bits per pixel (non-palletized)
- Supports one base layer (background)
- Supports two overlay layer windows
- Supports one high end overlay (HEO) window
- Supports one hardware cursor, fixed or free size
- Hardware cursor fixed size on the following patterns: 32 x 32, 64 x 64, and 128 x 128
- Little Endian Memory Organization

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- Programmable timing engine, with integer clock divider
- Programmable polarity for data, line synchro and frame synchro
- Display size up to 2048 x 2048 or up to 720 p in video format
- Color lookup table with up to 256 entries and predefined 8-bit Alpha
- Programmable negative and positive row striding for all layers
- Programmable negative and positive pixel striding for all overlay1, overlay2, and HEO Layers
- High-end overlay supports 4:2:0 planar mode and semi-planar mode
- High-end overlay supports 4:2:2 planar mode, semi-planar mode and packed
- High-end overlay includes chroma upsampling unit
- Horizontal and vertical rescaling unit with edge interpolation and independent non-integer ratio
- Hidden layer removal supported
- Integrates fully-programmable color space conversion
- Overlay1, Overlay2, and high-end Overlay Integrate Rotation Engine: 90, 180, 270
- Blender function supports arbitrary 8-bit alpha value and chroma keying
- DMA user interface uses linked list structure and add-to-queue structure

Table 11 shows the I/O lines description of the LCD bus.

Table 11: I/O lines description

Name	Description	Type
LCD_PWM	Contrast control signal using pulse width modulation	Output
LCD_HSYNC	Horizontal synchronization pulse	Output
LCD_VSYNC	Vertical synchronization pulse	Output
LCD_DAT[23:0]	LCD 24-bit data bus	Output
LCD_DEN	Data enable	Output
LCD_DISP	Display enable signal	Output
LCD_PCLK	Pixel clock	Output

9.3 Audio Interface (Synchronous Serial Controller)

The Synchronous Serial Controller (SSC) provides a synchronous communication link with external devices. It supports many serial synchronous communication protocols generally used in audio and telecom applications such as I2S, Short Frame Sync, and Long Frame Sync.

The SSC contains an independent receiver and transmitter and a common clock divider. Both the receiver and the transmitter interface with three signals:

- TD/RD signal for data
- TK/RK signal for the clock
- TF/RF signal for the Frame Sync.

The transfers can be programmed to start automatically or on different events detected on the Frame Sync signal.

Table 12: SSC I/O lines description

Name	Description	Type
RF	Receiver Frame Synchro	Input/Output
RK	Receiver Clock	Input/Output
RD	Receiver Data	Input
TF	Transmitter Frame Synchro	Input/Output
TK	Transmitter Clock	Input/Output
TD	Transmitter Data	Output

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Typical application block diagram of SSC bus is shown in Figure 6.

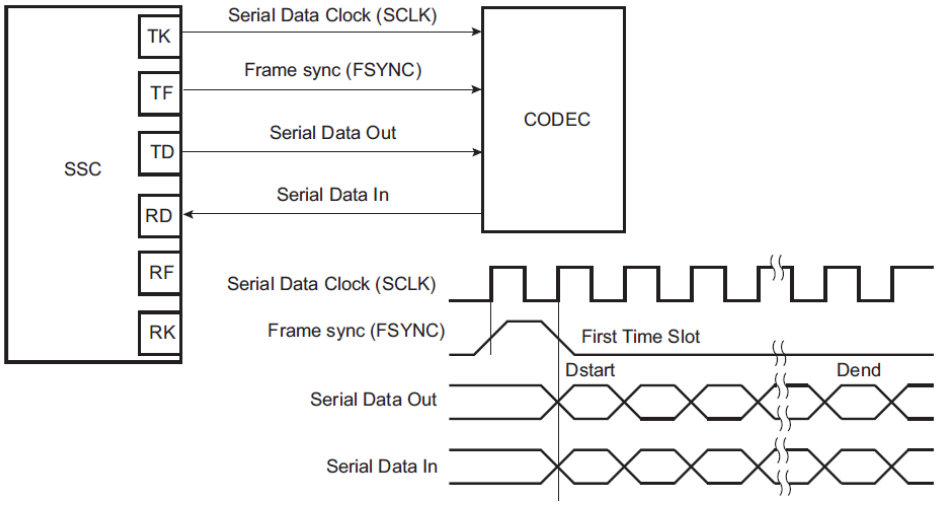

Figure 6: Typical application block diagram of SSC bus

9.4 High Speed Multimedia Card Interface

The high-speed Multimedia Card Interface (HSMCI) supports the MultiMedia Card (MMC) Specification V4.3, the SD memory card specification V2.0, and the SDIO V2.0 specification.

The SD memory card communication is based on a nine-pin interface (clock, command, four data, and three power lines) and the high-speed MMC on a seven-pin interface (clock, command, one data, three power lines, and one reserved for future use). The SD memory card interface also supports high-speed MMC operations. The main differences between SD and high-speed MultiMedia cards are the initialization process and the bus topology.

Table 13: HSMCI I/O lines description

Name	Description	Type	Comments
MCCDA	Command/Response	I/O/PP/OD	CMD of an MMC or SDCard/SDIO
MCCK	Clock	I/O	CLK of an MMC or SD Card/SDIO
MCDA0–MCDA7	Data 0..7	I/O/PP	DAT[0..7] of an MMC DAT[0..3] of an SD Card/SDIO

9.5 Serial Peripheral Interface (SPI)

The SPI system consists of two data lines and two control lines:

- Master Out/Slave In (SPI_MOSI) – This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In/Slave Out (SPI_MISO) – This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPI_CLK)—This control line is driven by the master and regulates the flow of the data bits. The master can transmit data at a variety of baud rates; there is one SPI_CLK pulse for each bit that is transmitted.
- Slave Select (SPI_NPCS)—This control line allows slaves to be turned on and off by hardware.

Table 14: SPI I/O lines descriptions

Name	Description	Type	
		Master	Slave
SPIx_MISO	Master in/Slave out	Input	Output

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Name	Description	Type	
		Master	Slave
SPIx_MOSI	Master out/Slave in	Output	Input
SPIx_CLK	Serial clock	Output	Input
SPIx_NPCS[1-3]	Peripheral chip selects	Output	Unused
SPI1_NPCS0	Peripheral chip select/slave select	Output	Input

Typical application block diagram of SPI bus is shown in Figure 7.

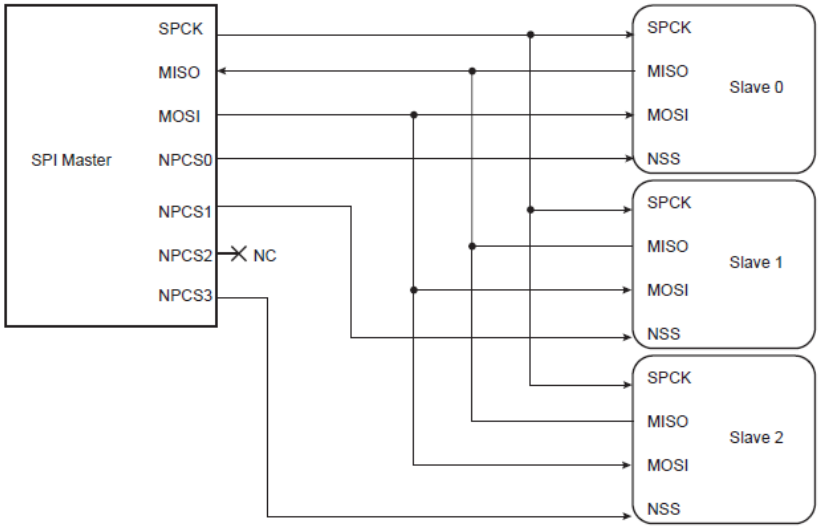

Figure 7: Typical application block diagram of SPI bus

9.6 Can Bus Interface

The CAN bus offers optimized features to support the Time Triggered Communication (TTC) protocol.

- Fully compliant with CAN 2.0 Part A and 2.0 Part B
- Bit rates up to one Mbit/second
- Eight object-oriented mailboxes with the following properties:
  - CAN Specification 2.0 Part A or 2.0 Part B programmable for each message
  - Object configurable in receive (with overwrite or not) or transmit modes
  - Independent 29-bit identifier and mask defined for each mailbox
  - 32-bit access to data registers for each mailbox data object
  - Uses a 16-bit timestamp on receive and transmit messages
  - Hardware concatenation of ID masked bitfields to speed up family ID processing
- 16-bit internal timer for timestamping and network synchronization
- Programmable reception buffer length up to eight mailbox objects
- Priority management between transmission mailboxes
- Autobaud and listening mode
- Low-power mode and programmable wake-up on bus activity or by the application
- Data, remote, error and overload frame handling
- Register write protection

Table 15: Can bus interface I/O lines description

Name	Description	Type
CAN_TX1	CAN Receive Serial Data	Input

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Name	Description	Type
CAN_RX1	CAN Transmit Serial Data	Output

9.7 Two-wire Interface (TWI)

The Atmel/Microchip two-wire interface (TWI) interconnects components on a unique two-wire bus. It is made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It can be used with any Atmel/Microchip two-wire interface bus Serial EEPROM and I²C compatible device such as a Real Time Clock (RTC), dot matrix/graphic LCD controllers, and temperature sensor. The TWI is programmable as a master or a slave with sequential or single-byte access. Multiple master capability is supported.

Table 16 lists the compatibility level of the Atmel/Microchip two-wire Interface in Master mode and a full I2C compatible device.

Table 16: Atmel/Microchip TWI compatibility with I2C standard

I²C Standard	Atmel/Microchip TWI
Standard mode speed (100 kHz)	Supported
Fast mode speed (400 kHz)	Supported
7- or 10-bit slave addressing	Supported
START byte(1)	Not Supported
Repeated start (Sr) condition	Supported
ACK and NACK management	Supported
Slope control and input filtering (fast mode)	Not Supported
Clock stretching/synchronization	Supported
Multi Master Capability	Supported

Note 1: START + b000000001 + Ack + Sr

Table 17: TWI I/O lines description

Name	Description	Type
TW_D	Two-wire Serial Data (drives external serial data line – SDA)	Input/Output
TW_CLK	Two-wire Serial Clock (drives external serial clock line – SCL)	Input/Output

9.8 Analog-to-Digital Converter (ADC)

There are six analog input channels available on the 60 SOM. The analog power supply (VDDANA) and the reference voltage (ADVREF) are set to 3.3V on the module. Analog inputs between these voltages (3.3V) convert to values based on a linear conversion. Software trigger, external trigger on rising edge of the ADTRG pin or internal triggers from Timer Counter output(s) are configurable.

Table 18: ADC I/O lines description

Name	Description	Type
AD0	Analog input channels (Upper-left touch panel)	Analog
AD1	Analog input channels (Upper-right touch panel)	Analog
AD2	Analog input channels (Lower-left touch panel)	Analog
AD3	Analog input channels (Lower-right touch panel)	Analog
AD4	Analog input channels (Panel input)	Analog
AD5	Analog input channels	Analog
ADTRG	External trigger	Input

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10 MECHANICAL SPECIFICATIONS

The 60 Series SOM measures 30 x 30 x 2.8 mm. Detail drawings are shown in Figure 8.

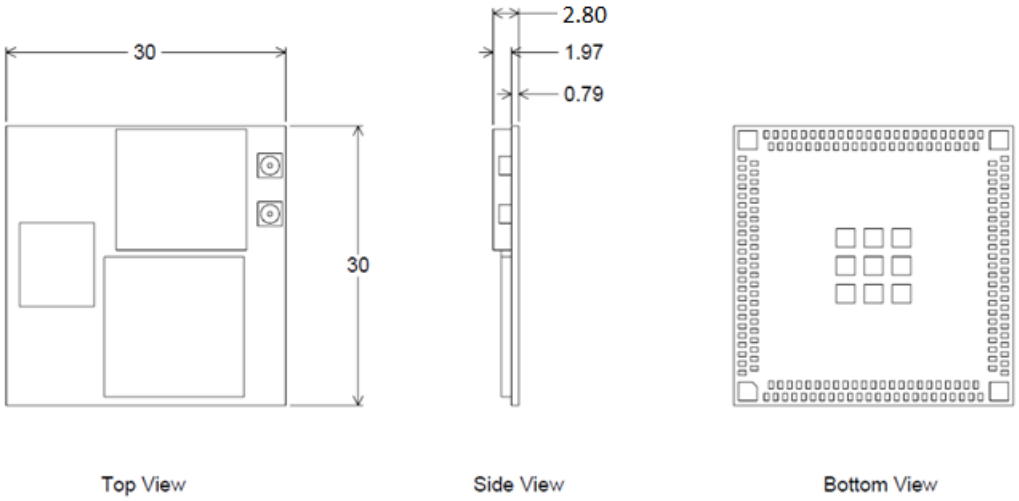

Figure 8: Module dimension of 60 SOM

Note: The Wi-Fi MAC address is located on the product label. The last digit of the Wi-Fi MAC address is assigned to end with either 0, 4, 8, or C. The BT MAC address is the Wi-Fi MAC address plus 3.

The 10/100 Ethernet LAN MAC (ELAN) address is also shown in the label on the 60 SOM. The other 10/100/1000 Giga-bits Ethernet LAN MAC address is the 10/100 Ethernet LAN MAC address plus 1.

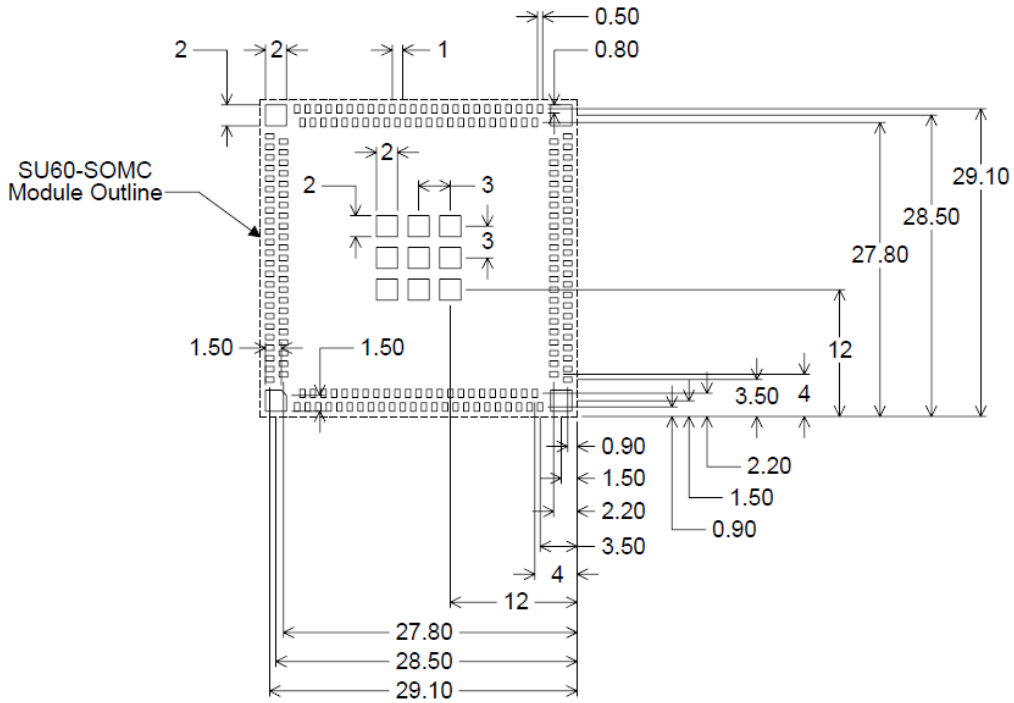

Figure 9: Mechanical drawing

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Recommended landing pad for the 60 SOM. More ground via and the use of 1-oz copper is recommended in our design to get better thermal dissipation.

Note: The stencil thickness should be ≥ 0.1 mm and adjust the opening size/ratio and the SMT reflow thermal profile accordingly to minimize the void (less than 30% according to IPC standard) in the landing pad as possible.

11 Assembly Instructions

11.1 Required Storage Conditions

11.1.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior*** to opening the dry packing:

- Normal temperature: 5~40℃
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity refers to *relative humidity*.

11.1.2 After Opening the Dry Packing

The following are required storage conditions ***after*** opening the dry packing (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5~25℃
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering

  Storage conditions following opening and prior to performing the 1st reflow:

  - Temperature: 5~25℃
  - Humidity: 60% or less
  - Period: 48 hours or less after opening

  Note: This module only allows one time reflow process. Applying more than one time reflow will cause damage.

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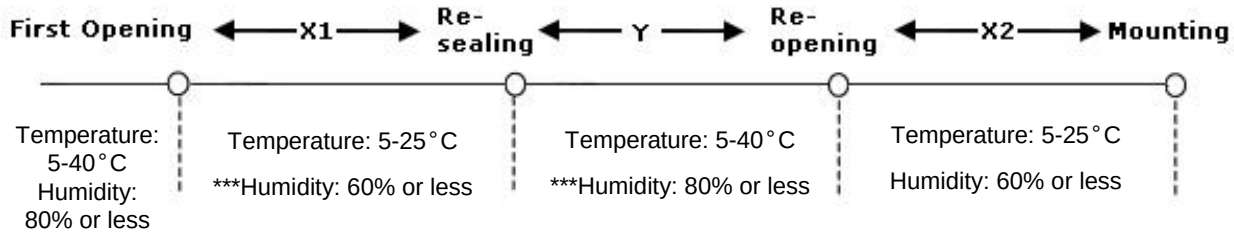
11.1.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Put the device back to dry packing immediately when it is not used.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

Storage temperature and humidity



*** - External atmosphere temperature and humidity of the dry packing

Storage period

- X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
- Y – Two weeks or less

11.2 Baking Conditions

Baking conditions and processes for the 60 SOM follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the 60 SOM must be mounted (according to **MSL4/Moisture Sensitivity Level 4)** within 72 hours at <30℃ and <60% relative humidity according to IPC/JEDEC J-STD -033C.
- If the 60 SOM is not mounted within 72 hours or if, when the packaging is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125℃ (±5℃).

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11.3 Surface Mount Conditions

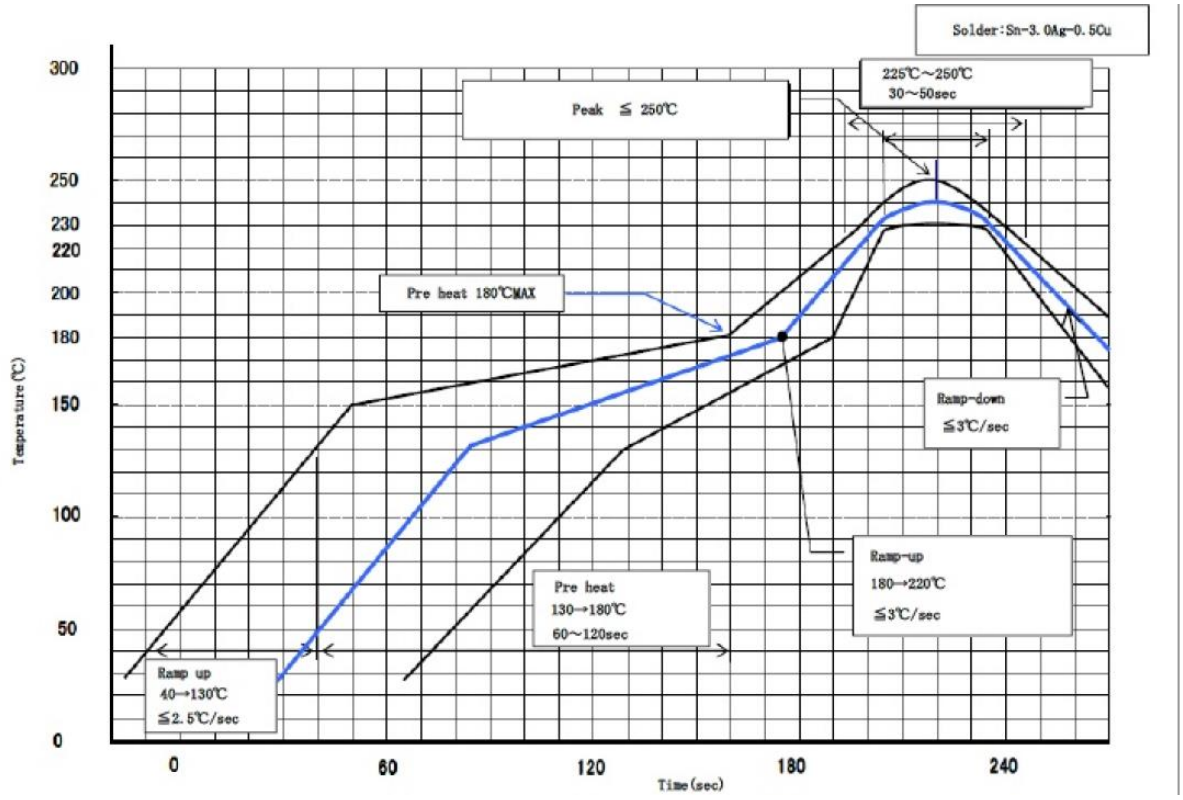
The following soldering conditions are recommended to ensure device quality. You must adjust for your platform PCB size, thickness of stencil, and the solder paste you use to get optimized solder quality.

11.3.1 Soldering

Convection reflows or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

Pin



Ramp-up : 40 - 130 deg. Less than 2.5 deg./sec

Pre heat : 130 - 180 deg. 60 - 120 sec , 180 deg. MAX

Ramp-up : 180 - 220 deg. Less than 3 deg./sec

Peak Temperature : MAX 250 deg.

225 deg. ~ 250 deg. , 30 ~ 50 sec

Ramp-down : Less than 3 deg./sec

Figure 10: Temperature profile for reference only, customer need to adjust this for their assembly condition

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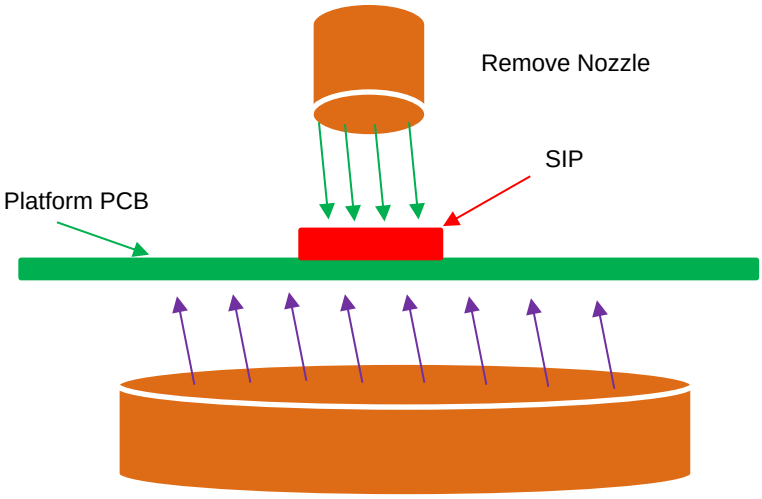
11.3.2 Cautions on Removing the 60 SOM from the Platform for RMA

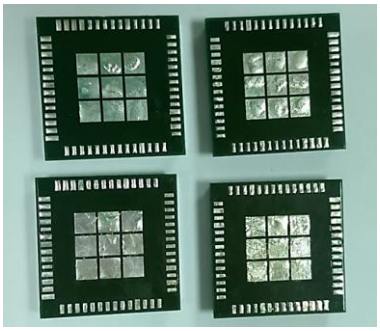
- Bake the platform before removing the Wi-Fi/BT SIP from the platform. Reference baking conditions.
- Remove the Wi-Fi/BT SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280°C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250°C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330°C). Heat the SIP until it can be removed from platform PCB.

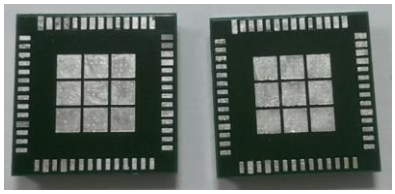


- Remove the residue solder under the bottom side of 60 SOM.



(Not accepted for RMA)

With residue solder on the bottom



(Accepted for RMA analysis)

Without residue solder on the bottom

- Remove and clean the residue flux is needed.

11.3.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.

The devices should be mounted within one year of the date of delivery.

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12 REGULATORY

12.1 Certified Antennas

Model	Type	Connector	2400~2483.5MHz 5150~5250MHz 5250~5350MHz 5470~5725MHz 5725~5850MHz
Laird/NanoBlade-IP04	PCB Dipole	IPEX U.FL	2 dBi (2.4-2.5 GHz), 3.9 dBi (5.15-5.35 GHz), 4 dBi (5.6 GHz)
Laird/MAF95310 Mini NanoBlade Flex	PCB Dipole	IPEX U.FL	2.79 dBi @ 2.4 GHz, 3.38 dBi @ 5 GHz
Ethertronics/WLAN_1000146	Magnetic Dipole	IPEX U.FL	2.5 dBi (2.390-2.490), 3.5 dBi (4.900-5.100), 3.5 dBi (5.150-5.350), 3.5 dBi (5.70-5.900)
LSR/FlexPIFA 001-0016	PIFA	IPEX U.FL	2.5 dBi @2.4 GHz, 3 dBi @5GHz
LSR/001-0009	Dipole	IPEX U.FL	2 dBi @2.4 GHz, 2 dBi @5GHz
FlexMIMO Antenna EFD2455A3S-10MHF1	PIFA	IPEX U.FL	2.5dBi@2.4GHz, 3dBi@5GHz

12.2 FCC and IC

Model	US/FCC	CANADA/IC
60 SOM	SQG-SU60SOMC	3147A-SU60SOMC

The 60 SOM is designed to pass certification with the antenna listed below. The required antenna impedance is 50 ohms.

Model	Type	Connector	Peak gain (dBi)				
			2400~2483.5 MHz	5150~5250 MHz	5250~5350 MHz	5470~5725 MHz	5725~5850 MHz
Laird/NanoBlade-IP04	PCB Dipole	IPEX U.FL	2.0 dBi	3.9 dBi	3.9 dBi	4.0 dBi	
Laird/MAF95310 Mini NanoBlade Flex	PCB Dipole	IPEX U.FL	2.79 dB	3.38 dBi			
Ethertronics/WLAN_1000146	Magnetic Dipole	IPEX U.FL	2.5 dBi	3.5 dBi			
LSR/FlexPIFA 001-0016	PIFA	IPEX U.FL	2.5 dBi	3.0 dBi			
LSR/001-0009	Dipole	IPEX U.FL	2.0 dBi	2.0 dBi			
FlexMIMO Antenna EFD2455A3S-10MHF1	PIFA	IPEX U.FL	2.5 dBi	3.0dBi			

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12.2.1 FCC

Federal Communication Commission Interference Statement

This equipment was tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Important Note

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body.

This transmitter must not be co-located or operated in conjunction with any other antenna or transmitter.

Country Code selection feature to be disabled for products marketed to the US/CANADA.

This device is intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20 centimeters is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna,
3. For all products market in US, OEM must limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change.

If the conditions above are met, further transmitter test are not required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Important Note

In the event that these conditions cannot be met (for example, certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator is responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in a device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: **Contains FCC ID: SQG-SU60SOMC**.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

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12.2.2 Industry Canada

Industry Canada Statement

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

- This device may not cause interference; and
- This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient des émetteurs / récepteurs exempts de licence qui sont conformes au (x) RSS (s) exemptés de licence d'Innovation, Sciences et Développement économique Canada. L'opération est soumise aux deux conditions suivantes:

- *Cet appareil ne doit pas causer d'interférences*
- *Cet appareil doit accepter toute interférence, y compris les interférences pouvant provoquer un fonctionnement indésirable de l'appareil*

This radio transmitter (IC: 3147A-SU60SOMC) has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio (IC: 3147A-SU60SOMC) a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Antenna Information

Model	Type	Connector	Peak gain (dBi)				
			2400~2483.5 MHz	5150~5250 MHz	5250~5350 MHz	5470~5725 MHz	5725~5850 MHz
Laird/NanoBlade-IP04	PCB Dipole	IPEX U.FL	2.0 dBi	3.9 dBi	3.9 dBi	4.0 dBi	
Laird/MAF95310 Mini NanoBlade Flex	PCB Dipole	IPEX U.FL	2.79 dB	3.38 dBi			
Ethertronics/WLAN_1000146	Magnetic Dipole	IPEX U.FL	2.5 dBi	3.5 dBi			
LSR/FlexPIFA 001-0016	PIFA	IPEX U.FL	2.5 dBi	3.0 dBi			
LSR/001-0009	Dipole	IPEX U.FL	2.0 dBi	2.0 dBi			
Laird MIMO FlexPIFA Antenna EFD2455A3S-10MHF1	PIFA	IPEX U.FL	2.5 dBi	3.0 dBi			

Caution:

(i) The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

(ii) for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;

(iii) for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate; and

Operations in the 5.25-5.35GHz band are restricted to indoor usage only.

Avertissement:

(i) les dispositifs fonctionnant dans la bande de 5150 à 5250MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;

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(ii) pour les dispositifs munis d'antennes amovibles, le gain maximal d'antenne permis pour les dispositifs utilisant les bandes de 5250 à 5350MHz et de 5470 à 5725 MHz doit être conforme à la limite de la p.i.r.e;

(iii) pour les dispositifs munis d'antennes amovibles, le gain maximal d'antenne permis (pour les dispositifs utilisant la bande de 5725 à 5850 MHz) doit être conforme à la limite de la p.i.r.e. spécifiée pour l'exploitation point à point et l'exploitation non point à point, selon le cas;

Les opérations dans la bande de 5.25-5.35GHz sont limités à un usage intérieur seulement.

Radiation Exposure Statement

This equipment complies with Canada radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

Déclaration d'exposition aux radiations

Cet équipement est conforme Canada limites d'exposition aux radiations dans un environnement non contrôlé. Cet équipement doit être installé et utilisé à distance minimum de 20cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following condition:

- The transmitter module may not be co-located with any other transmitter or antenna.

As long as the condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:

- *Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.*

Tant que les 1 condition ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator is responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

Note Importante:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

The final end product must be labeled in a visible area with the following: ***Contains IC:*** 3147A-SU60SOMC

Plaque signalétique du produit final

Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: ***Contient des IC:*** 3147A-SU60SOMC

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

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Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

12.3 European Union Regulatory

The 60 Series SOM has been tested for compliance with relevant standards for the EU market. 60 SOM module was tested with antennas listed below.

Model	Type	Connector	2400~2483.5MHz 5150~5250MHz 5250~5350MHz 5470~5725MHz 5725~5850MHz
Laird/NanoBlade-IP04	PCB Dipole	IPEX U.FL	2 dBi (2.4-2.5 GHz), 3.9 dBi (5.15-5.35 GHz), 4 dBi (5.6 GHz)
Laird/MAF95310 Mini NanoBlade Flex	PCB Dipole	IPEX U.FL	2.79 dBi @ 2.4 GHz, 3.38 dBi @ 5 GHz
Ethertronics/WLAN_1000146	Magnetic Dipole	IPEX U.FL	2.5 dBi (2.390-2.490), 3.5 dBi (4.900-5.100), 3.5 dBi (5.150-5.350),3.5 dBi (5.70-5.900)
LSR/FlexPIFA 001-0016	PIFA	IPEX U.FL	2.5 dBi @ 2.4GHz, 3 dBi @ 5GHz
LSR/001-0009	Dipole	IPEX U.FL	2 dBi @ 2.4 GHz, 2 dBi @ 5 GHz
MIMO FlexPIFA Antenna EFD2455A3S-10MHF1	PIFA	IPEX U.FL	2.5dBi@2.4GHz, 3dBi@5GHz

The OEM should consult with a qualified test house before entering their device into an EU member country to make sure all regulatory requirements have been met for their complete device.

Reference the Declaration of Conformities listed below for a full list of the standards that the modules were tested to. Test reports are available upon request.

12.3.1 EU Declarations of Conformity

Manufacturer:	Laird
Products:	60 SOM series
EU Directives:	1999/5/EC – R&TTE 2006/95/EC – Low Voltage directive (LVD) 2004/108/EC – Electromagnetic compatibility (EMC) 2014/30/EU – EMC
Conformity Assessment:	Annex IV

Reference standards used for presumption of conformity:

Article Number	Requirement	Reference standard(s)
3.1a	2006/95/EC Low voltage equipment safety	EN 60950-1:2006+A11:2009+A1:2010+A12:2011+A2:2013
	2006/95/EC RF Exposure	EN 62311:2008
3.1b	2004/108/EC Protection requirements with respect to electromagnetic compatibility	EN 301 489-1 v1.9.2 (2011-09) EN 301 489-17 v2.2.1 (2012-09)
3.2	1999/5/EC Means of the efficient use of the radio frequency spectrum	EN 300 328 v1.9.1 (2015-02) EN 301 893 v1.8.1(2015-03)

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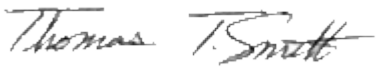
Declaration:

We, Laird, declare under our sole responsibility that the essential radio test suites have been carried out and that the above product to which this declaration relates is in conformity with all the applicable essential requirements of Article 3 of the EU Directive 1999/5/EC, when used for its intended purpose.

Place of Issue:	Laird W66N220 Commerce Court, Cedarburg, WI 53012 USA tel: +1-262-375-4400 fax: +1-262-364-2649
Date of Issue:	TBD
Name of Authorized Person:	Thomas T Smith, Director of EMC Compliance
Signature of Authorized Person:	

13 Ordering Information

Part Number	Description
453-00003	60 Series SOM
455-00003	Development board for the 60 Series SOM
455-00004	LCD Touchscreen for the 60 Series SOM development board (add-on)

13.1 General Comments

This is a preliminary datasheet. Please check with Laird for the latest information before commencing a design. If in doubt, ask.

cs **Česky [Czech]**	*[Jméno výrobce]* tímto prohlašuje, že tento *[typ zařízení]* je ve shodě se základními požadavky a dalšími příslušnými ustanoveními směrnice 1999/5/ES.
da **Dansk [Danish]**	Undertegnede *[fabrikantens navn]* erklærer herved, at følgende udstyr *[udstyrets typebetegnelse]* overholder de væsentlige krav og øvrige relevante krav i direktiv 1999/5/EF.
de **Deutsch [German]**	Hiermit erklärt *[Name des Herstellers]*, dass sich das Gerät *[Gerätetyp]* in Übereinstimmung mit den grundlegenden Anforderungen und den übrigen einschlägigen Bestimmungen der Richtlinie 1999/5/EG befindet.
et **Eesti [Estonian]**	Käesolevaga kinnitab *[tootja nimi = name of manufacturer]* seadme *[seadme tüüp = type of equipment]* vastavust direktiivi 1999/5/EÜ põhinõuetele ja nimetatud direktiivist tulenevatele teistele asjakohastele sätetele.
en **English**	Hereby, *[name of manufacturer]*, declares that this *[type of equipment]* is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.
es **Español [Spanish]**	Por medio de la presente *[nombre del fabricante]* declara que el *[clase de equipo]* cumple con los requisitos esenciales y cualesquiera otras disposiciones aplicables o exigibles de la Directiva 1999/5/CE.
el **Ελληνική [Greek]**	ΜΕ ΤΗΝ ΠΑΡΟΥΣΑ *[name of manufacturer]* ΔΗΛΩΝΕΙ ΟΤΙ *[type of equipment]* ΣΥΜΜΟΡΦΩΝΕΤΑΙ ΠΡΟΣ ΤΙΣ ΟΥΣΙΩΔΕΙΣ ΑΠΑΙΤΗΣΕΙΣ ΚΑΙ ΤΙΣ ΛΟΙΠΕΣ ΣΧΕΤΙΚΕΣ ΔΙΑΤΑΞΕΙΣ ΤΗΣ ΟΔΗΓΙΑΣ 1999/5/ΕΚ.
fr **Français [French]**	Par la présente *[nom du fabricant]* déclare que l'appareil *[type d'appareil]* est conforme aux exigences essentielles et aux autres dispositions pertinentes de la directive 1999/5/CE.
it **Italiano [Italian]**	Con la presente *[nome del costruttore]* dichiara che questo *[tipo di apparecchio]* è conforme ai requisiti essenziali ed alle altre disposizioni pertinenti stabilite dalla direttiva 1999/5/CE.
Latviski [Latvian]	Aršo*[name of manufacturer /izgatavotājanosaukums]* deklarē, ka*[type of equipment / iekārtas tips]*atbilstDirektīvas 1999/5/EK būtiskajāmprasībām un citiemar to saistītajiemnoteikumiem.

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Lietuvių [Lithuanian]	Šiuo *[manufacturer name]* deklaruoja, kad šis *[equipment type]* atitinka esminius reikalavimus ir kitas 1999/5/EB Direktyvos nuostatas.
Nederlands [Dutch]	Hierbij verklaart *[naam van de fabrikant]* dat het toestel *[type van toestel]* in overeenstemming is met de essentiële eisen en de andere relevante bepalingen van richtlijn 1999/5/EG.
Malti [Maltese]	Hawnhekk, *[isem tal-manifattur]*, jiddikjara li dan *[il-mudel tal-prodott]* jikkonforma mal-ħtiġijiet essenzjali u ma provvedimenti oħrajn relevanti li hemm fid-Dirrettiva 1999/5/EC.
Magyar [Hungarian]	Alulírott, *[gyártó neve]* nyilatkozom, hogy a *[... típus]*megfelel a vonatkozó alapvetõ követelményeknek és az 1999/5/EC irányelv egyéb elõírásainak.
Polski [Polish]	Niniejszym *[nazwa producenta]* oświadcza, że *[nazwa wyrobu]* jest zgodny z zasadniczymi wymogami oraz pozostałymi stosownymi postanowieniami Dyrektywy 1999/5/EC.
Português [Portuguese]	*[Nome do fabricante]* declara que este *[tipo de equipamento]* está conforme com os requisitos essenciais e outras disposições da Directiva 1999/5/CE.
Slovensko [Slovenian]	*[Ime proizvajalca]* izjavlja, da je ta *[tip opreme]* v skladu z bistvenimi zahtevami in ostalimi relevantnimi določili direktive 1999/5/ES.
Slovensky [Slovak]	*[Menovýrobcu]*týmtovyhlasuje, že*[typzariadenia]*spĺňazákladnépožiadavky a všetkypríslušnéustanoveniaSmernice 1999/5/ES.
Suomi [Finnish]	*[Valmistaja = manufacturer]* vakuuttaa täten että *[type of equipment = laitteen tyyppimerkintä]* tyyppinen laite on direktiivin 1999/5/EY oleellisten vaatimusten ja sitä koskevien direktiivin muiden ehtojen mukainen.
Svenska [Swedish]	Härmed intygar *[företag]* att denna *[utrustningstyp]* står I överensstämmelse med de väsentliga egenskapskrav och övriga relevanta bestämmelser som framgår av direktiv 1999/5/EG.

13.1.1 Labeling Requirements

The final end product must be labeled in a visible area with the following notice:

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